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GATE NOISE IN MOS FET'S AT MODERATELY HIGH FREQUENCIES

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Abstract—A lumped model approach is used to evaluate the drain noise, gate noise and correlation between gate and drain noise for an *n*-channel enhancement MOS field-effect transistor. Effects of the substrate resistivity are examined in detail. It is found that as the substrate doping increases, the correlation coefficient increases over the value of 0·395 for an intrinsic substrate. This conclusion is in direct disagreement with previously published results.

Résumé—On approche le problème à l'aide d'un modèle aggloméré pour évaluer le bruit de déversement, le bruit du circuit à déclenchement périodique et la corrélation entre les bruits du circuit à déclenchement périodique et du déversement pour un transistor à *n*-canaux à effet de champ MOS de réhaussement. On examine en détail les effets sur la résistivité de la base. On trouve qu'à mesure que le doping de la base accroit, le coefficient de corrélation augmente au-dessus de la valeur de 0,395 pour une base intrinsèque. Cette conclusion est en désaccord direct avec les résultats précédemment publiés.

Zusammenfassung—Ein Modell mit konzentrierten Elementen wird benutzt, um das Drain- und Gaterauschen und deren Korrelation in einem *n*-Kanal-Anreicherungs-MOS-Feldeffekttransistor zu erklären. Der Einfluß der Substratleitfähigkeit wird im einzelnen untersucht. Daher ergibt sich mit zunehmender Substratdotierung eine Zunahme des Korrelationskoeffizienten über Werte von 0,395 hinaus, der für ein eigenleitendes Substrat gilt. Diese Folgerung ist in direktem Widerspruch mit früher veröffentlichten Resultaten.

1. INTRODUCTION

THE EFFECTS of fixed bulk charge on the thermal noise characteristics of MOS FET's have been analyzed in detail by Sah *et al.*[1] and the effects of the substrate doping on the gate noise have been presented by Rao[2].

An alternative approach using circuit analysis techniques, first introduced by Sah[3], and recently used by Fu and Sah[4], yields identical results for the thermal noise. The technique is utilized to calculate the gate noise and correlation coefficient in the pre pinch-off mode.

The FET with both drain and gate a.c. short-circuited to the source can be split at a point x in the channel as shown in Figs. 1(a) and 1(b). Using the small signal equivalent circuit for the bulk charge model[5], it can be shown that the resistances R_l and R_r are given by

$$R_l = \frac{1}{g_{ol}} \tag{1}$$

$$R_r = \frac{1}{g_{or} + g_{mr} + g_{mbr}} \tag{2}$$

where g_{ol} = output conductance for the transistor of channel length x
g_{or} = output conductance for the transistor of channel length $(L-x)$
g_{mr}, g_{mbr} = gate and substrate transconductances, respectively for the transistor of channel length $(L-x)$.

If the channel potential with respect to the source at the point x in the channel is denoted as V, then for the transistor of channel length $(L-x)$, the effective gate-source bias is $V_{gs}-V$, the drain-source bias is $V_{ds}-V$, and the substrate-source bias is $-V$. It is then easy to show that

$$\frac{1}{R_l} = -\frac{\mu_n Z}{x} Q_n \tag{3}$$

$$\frac{1}{R_r} = -\frac{\mu_n Z}{L-x} Q_n \tag{4}$$

where

$$Q_n = C_{ox}\left\{V_B\left(1+\frac{V}{2\phi_F}\right)^{1/2} - (V_{gs}-V_T+V_B-V)\right\} \tag{5}$$

μ_n = electron mobility in the channel
C_{ox} = oxide capacitance per unit area
x = co-ordinate defined in Fig. 1
V_T = threshold voltage, positive for an n-channel FET
Z = device breadth
L = channel length

and

$$V_B = \left[\frac{4qN_a\epsilon_s\phi_F}{C_{ox.}^2}\right]^{1/2} \tag{6}$$

where

q = magnitude of the electronic charge
N_a = substrate impurity concentration
ϵ_s = semiconductor permittivity
ϕ_F = Fermi potential in the p-type substrate.

The inversion charge Q_n is assumed to exist as a surface charge at the oxide-semiconductor interface, so that the thermal noise voltage $dv_n(x)$ generated in an element of channel of length dx at x may be calculated directly from the Nyquist theorem, and is given by

$$\overline{dv_n(x)^2} = -\frac{4kT\Delta f dx}{\mu_n Z Q_n}. \tag{7}$$

Neglecting the capacitances C_l and C_r in Fig. 1(b),

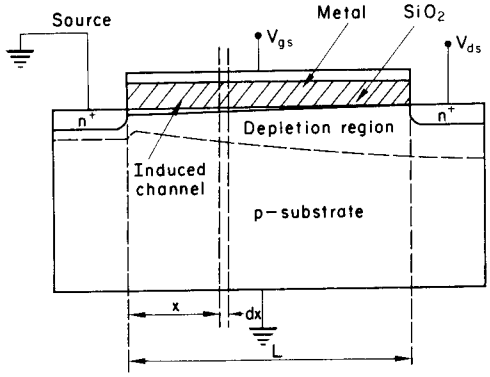

Fig. 1(a). Schematic representation of the MOS FET.

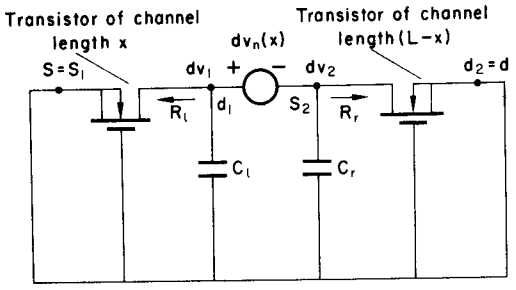

Fig. 1(b). The two-transistor equivalent circuit of a single FET of channel length L.

the contribution to the short-circuited drain noise current is

$$\overline{di_d^2} = \frac{\overline{dv_n(x)^2}}{(R_l+R_r)^2} = \frac{4kT\Delta f}{I_d}\left(\frac{\mu_n Z}{L}\right)^2 Q_n^2 dV. \tag{8}$$

This follows from the well-known expression for the drain current

$$I_d = -\mu_n Z Q_n \frac{dV}{dx}. \tag{9}$$

Integration of (8) from $V=0$ at the source to $V=V_{ds}$ at the drain yields

$$\overline{i_d^2} = \frac{4kT\Delta f}{I_d}\left(\frac{\mu_n Z C_{ox}}{L}\right)^2 K \tag{10}$$

where

$$K = \int_0^{V_{ds}} \left(\frac{Q_n}{C_{ox}}\right)^2 dV$$

$$= \frac{1}{3}\left\{3V_B^2 V_{ds}\left(1+\frac{V_{ds}}{4\phi_F}\right) + (V_{gs}-V_T+V_B)^3 - (V_{gs}-V_T+V_B-V_{ds})^3 - 8\phi_F V_B(V_{gs}-V_T+V_B+2\phi_F)\left[\left(1+\frac{V_{ds}}{2\phi_F}\right)^{3/2}-1\right] + \frac{48}{5}\phi_F^2 V_B\left[\left(1+\frac{V_{ds}}{2\phi_F}\right)^{5/2}-1\right]\right\} \tag{11}$$

and I_d is found by integrating (9) between $x = 0$ and $x = L$ so that

$$I_d = \frac{\mu_n C_{ox} Z}{L}\theta \tag{12}$$

where

$$\theta = V_{ds}(V_{gs} - V_T + V_B) - \frac{V_{ds}^2}{2} - \frac{4}{3}\phi_F V_B\left[\left(1+\frac{V_{ds}}{2\phi_F}\right)^{3/2} - 1\right].$$

Equation (10) can then be shown to yield results which are identical to those presented by Sah *et al.* [1].

A straightforward calculation of the gate noise $\overline{i_g^2}$ can be performed by considering the effects of C_l and C_r shown in Fig. 1. Assuming that capacitive currents to the gate are small compared with conductive current in the channel, it follows immediately that the noise voltage at d_1 is given by

$$\mathrm{d}v_1 = \mathrm{d}i_d R_l \tag{13}$$

and at s_2

$$\mathrm{d}v_2 = -\mathrm{d}i_d R_r. \tag{14}$$

Then the current flowing in the gate lead due to capacitive coupling between the channel and gate is given by

$$\mathrm{d}i_g = -[\mathrm{d}v_n(x)]j\omega\left[C_l\left(\frac{x}{L}\right) - C_r\left(\frac{L-x}{L}\right)\right] \tag{15}$$

where C_l is the gate-drain capacitance for the transistor of channel length x, and C_r is the gate-source capacitance for the transistor of channel length $(L-x)$. The total gate capacitance C_{gg} is given by

$$C_{gg} = C_{gs} + C_{gd} + C_{gb} = \frac{\partial Q_g}{\partial V_{gs}} \tag{16}$$

where C_{gs}, C_{gd} and C_{gb} are the gate-source, gate-drain and gate-bulk capacitances respectively. It can then be shown that

$$C_{gs} = \frac{\partial Q_g}{\partial V_{gs}} + \frac{\partial Q_g}{\partial V_{bs}} + \frac{\partial Q_g}{\partial V_{ds}} \tag{17}$$

and

$$C_{gd} = -\frac{\partial Q_g}{\partial V_{ds}}. \tag{18}$$

The capacitance C_l is found substituting V for V_{ds} in (18). Similarly, C_r is found by replacing V_{ds}, V_{gs} and V_{bs} by $(V_{ds}-V)$, $V_{gs}-V$) and $-V$ respectively in (17). This leads to

$$C_l = C_{ox} Z L\left(\frac{x}{L}\right) f_1(V, V_{gs}) \tag{19}$$

$$C_r = C_{ox} Z L\left(\frac{L-x}{L}\right) f_2(V, V_{gs}, V_{ds}) \tag{20}$$

where

$$f_1(V, V_{gs}) = -\left\{\frac{\Gamma}{(\theta_1)^2}\int_0^V \Gamma V \mathrm{d}V + \frac{\Gamma V}{\theta_1}\right\} \tag{21}$$

and

$$f_2(V, V_{gs}, V_{ds}) = \left\{1 - \frac{V_{ds2}}{\theta_2}\left(\frac{V_{ds2}}{2} - \Gamma_d\right) - \frac{1}{(\theta_2)^2}(V_{ds2} - \Gamma_d)\int_0^{V_{ds2}} \Gamma V \mathrm{d}V + \frac{V_B}{(\theta_2)^2}\left[\left(1+\frac{V_{ds}}{2\phi_F}\right)^{1/2} - \left(1+\frac{V}{2\phi_F}\right)^{1/2}\right]\cdot \left[(V_{gs2} - V_T + V_B)\int_0^{V_{ds2}} \Gamma \mathrm{d}V - \int_0^{V_{ds2}} \Gamma V \mathrm{d}V\right] + \frac{V_B}{4\phi_F\theta_2}\left[(V_{gs2} - V_T + V_B)\int_0^{V_{ds2}} \frac{\mathrm{d}V}{\left(1 - \frac{V_{bs}}{2\phi_F} + \frac{V}{2\phi_F}\right)^{1/2}} - \int_0^{V_{ds2}} \frac{V \mathrm{d}V}{\left(1 - \frac{V_{bs}}{2\phi_F} + \frac{V}{2\phi_F}\right)^{1/2}}\right]\right\} \tag{22}$$

where

$$V_{ds2} = V_{ds} - V \tag{23}$$

$$V_{gs2} = V_{gs} - V \tag{24}$$

$$\Gamma = Q_n / C_{ox} \tag{25}$$

$$\Gamma_d = V_B\left(1+\frac{V_{ds}}{2\phi_F}\right)^{1/2} - (V_{gs}-V_T+V_B-V_{ds}). \quad (26)$$

In addition, it is easy to show that

$$\frac{x}{L} = \frac{\theta_1}{\theta} \quad (27)$$

$$\frac{L-x}{L} = \frac{\theta_2}{\theta} \quad (28)$$

where

$$\theta_1 = V(V_{gs}-V_T+V_B) - \frac{V^2}{2} - \frac{4}{3}\phi_F V_B\left[\left(1+\frac{V}{2\phi_F}\right)^{3/2} - 1\right] \quad (29)$$

$$\theta_2 = V_{ds2}(V_{gs2}-V_T+V_B) - \frac{1}{2}V_{ds2}^2 - \frac{4}{3}\phi_F V_B\left[\left(1+\frac{V_{ds}}{2\phi_F}\right)^{3/2} - \left(1+\frac{V}{2\phi_F}\right)^{3/2}\right]. \quad (30)$$

The integrals in (21) and (22) are performed in a straightforward manner using (5). Those with upper limit V_{ds2} must have V_{gs2} substituted for V_{gs} and V_{bs2} substituted for V_{bs} in the final results as well, where $V_{bs2} = -V$.

The gate noise is obtained from

$$\overline{i_g^2} = \int_0^{V_{ds}} \overline{di_g^* di_g} \quad (31)$$

and utilizing (5), (13) and (17) to (28) yields

$$\overline{i_g^2} = \frac{2kT\Delta f\omega^2 C_{ox} Z L^3}{\mu_n \phi_F \left(\frac{\theta}{(2\phi_F)^2}\right)^5} \int_0^{V_{ds}/2\phi_F} Y^2 d\left(\frac{V}{2\phi_F}\right) \quad (32)$$

where

$$Y = \frac{1}{(2\phi_F)^4}[(\theta_1)^2 f_1(V, V_{gs}) - (\theta_2)^2 f_2(V, V_{gs}, V_{ds})]. \quad (33)$$

The integral in (32) can be performed numerically. Graphs of the normalized gate noise are shown in Fig. 2 as a function of drain bias for various gate voltages in excess of the threshold voltage V_T. It should be noted that the terms $V_{p1}/2\phi_F$, $V_{p2}/2\phi_F$ and $V_{p3}/2\phi_F$ represent the normalized pinch-off potentials for the curves with $(V_{gs}-V_T)/2\phi_F = 4$, 6 and 8 respectively.

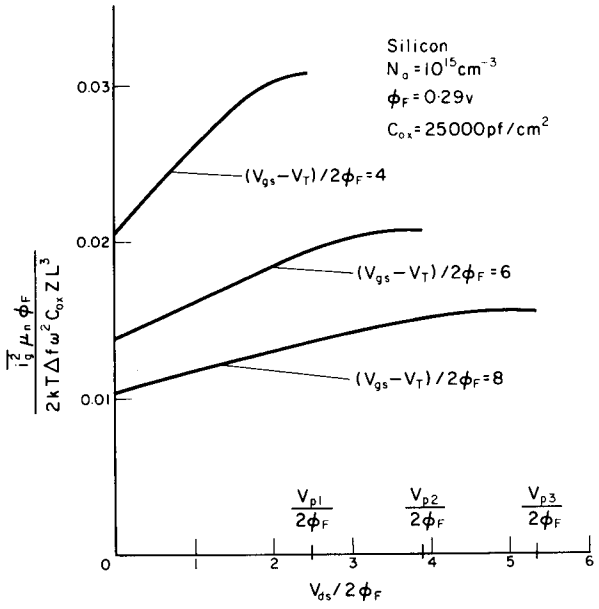

Fig. 2. Normalized gate noise for values of drain voltage ranging from zero to pinch-off.

The correlation coefficient c is easily obtained by considering the definition

$$c = jc_I = \frac{\overline{i_g^* i_d}}{[\overline{i_g^2}.\overline{i_d^2}]^{1/2}} \tag{34}$$

where c_I represents the magnitude of c.
Utilizing (8) and (15), it can be shown that

$$\overline{i_g^* i_d} = \frac{-j\omega 4kT\Delta f C_{ox} ZL}{\left(\frac{\theta}{(2\phi_F)^2}\right)^3} \int_0^{V_{ds}/2\phi_F} \frac{\Gamma}{2\phi_F} Y \mathrm{d}\left(\frac{V}{2\phi_F}\right). \tag{35}$$

Combining (10), (32), (34) and (35), the correlation coefficient can be written in integral form as

$$c = j \frac{-\int_0^{V_{ds}/2\phi_F} \left(\frac{\Gamma}{2\phi_F}\right) Y \mathrm{d}\left(\frac{V}{2\phi_F}\right)}{\left[\int_0^{V_{ds}/2\phi_F} Y^2 \mathrm{d}\left(\frac{V}{2\phi_F}\right) \int_0^{V_{ds}/2\phi_F} \left(\frac{\Gamma}{2\phi_F}\right)^2 \mathrm{d}\left(\frac{V}{2\phi_F}\right)\right]^{1/2}}. \tag{36}$$

The magnitude of c is given in Fig. 3 for bias conditions corresponding to those used in Fig. 2. Again, results were obtained using numerical techniques.

For an intrinsic substrate, $\phi_F \to 0$ and it can be shown that with the drain in saturation,

$$\theta_1 = V\left(V_p - \frac{V}{2}\right) \tag{37}$$

$$\theta_2 = \frac{1}{2}(V_p - V)^2 \tag{38}$$

$$\Gamma = V - V_p \tag{39}$$

$$f_1(V, V_{gs}) = \frac{1}{6} \frac{(V - V_p)(V - 3V_p)}{\left(V_p - \frac{V}{2}\right)^2} \tag{40}$$

and

$$f_2(V, V_{gs}, V_p) = \frac{2}{3} \tag{41}$$

where V_p = drain-source pinch-off potential.
The drain noise integral given by (11) reduces to

$$K = \frac{1}{3} V_p^3 \tag{42}$$

so that the drain noise expression given by (10)

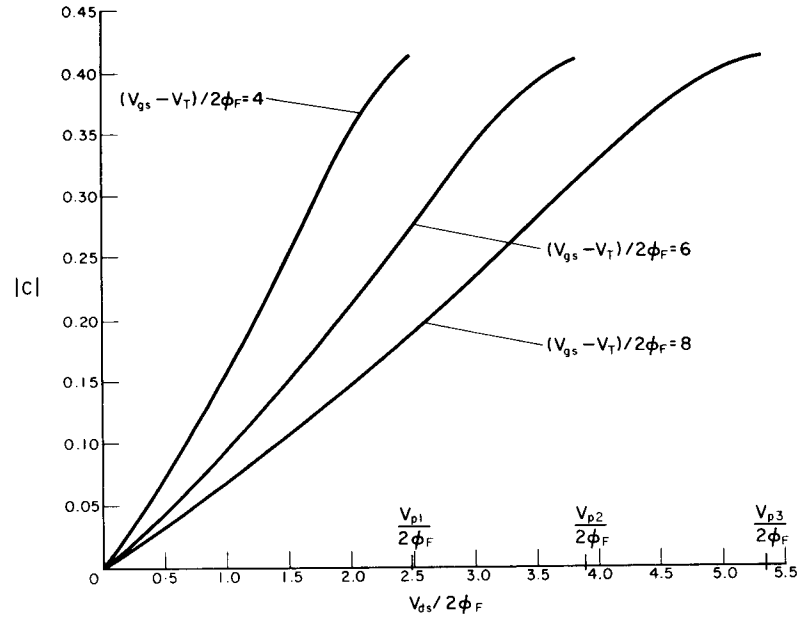

Fig. 3. Magnitude of the correlation coefficient for values of drain voltage ranging from zero to pinch-off.

reduces to

$$\overline{i_{do}^2} = \frac{8}{3} kT\Delta f g_{ms} \tag{43}$$

where

$$g_{ms} = \frac{\mu_n Z C_{ox} V_p}{L}. \tag{44}$$

The use of (37) to (41) in (33) yields

$$Y = \frac{V_p^6}{6}(V - V_p)(V_p - 3V). \tag{45}$$

The gate noise at pinch-off is then obtained by substitution into (34), giving

$$\overline{i_{go}^2} = \frac{64}{135} \frac{kT\Delta f \omega^2 (C_{ox} Z L)^2}{g_{ms}}. \tag{46}$$

In addition, (35) and (36) reduce to

$$\overline{i_{go}^* i_{do}} = -\frac{4}{9} kT\Delta f j\omega C_{ox} L Z \tag{47}$$

and

$$c = \frac{j}{4}\sqrt{\frac{5}{2}}. \tag{48}$$

Equations (43), (46), (47) and (48) are identical to those presented by Shoji[6] and Halladay and van der Ziel[7] for an intrinsic substrate.

The variations in $\overline{i_g^2}/\overline{i_{go}^2}$, $\overline{i_g^* i_d}/\overline{i_{go}^* i_{do}}$, and $|c|$ with substrate doping are given in Figs. 4, 5 and 6 respectively. The results for the gate noise and

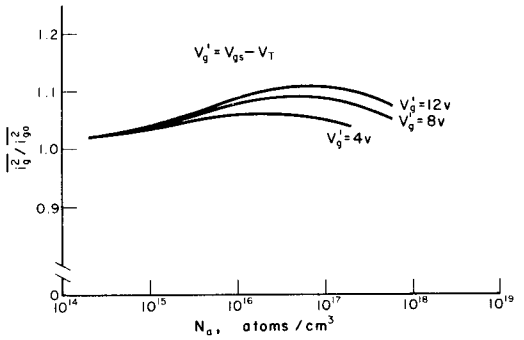

Fig. 4. Gate noise as a function of substrate doping at pinch-off, normalized to results obtained with $\phi_F = 0$.

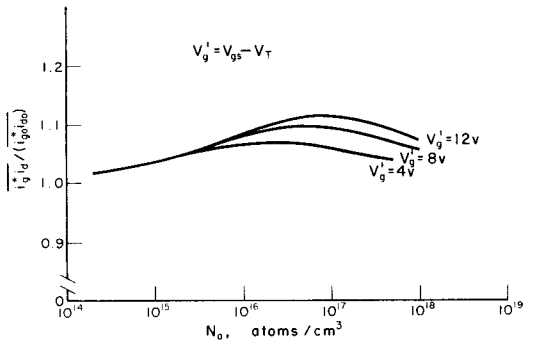

Fig. 5. Cross-correlation as a function of substrate doping at pinch-off, normalized to results obtained with $\phi_F = 0$.

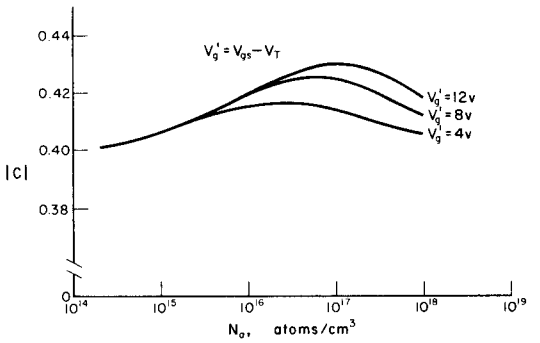

Fig. 6. Magnitude of the correlation coefficient as a function of substrate doping at pinch-off.

correlation term are similar in magnitude and form to those presented by Rao[2]. However, the magnitude of the correlation coefficient is in strong disagreement with his data. Rao states that $|c|$ decreases monotonically with increasing N_a, as a result of the variation of $\overline{i_d^2}$. Halladay and van der Ziel[7] have performed high frequency noise measurements on MOS FET's and have found that $|c|$ increases over its value of 0·395 given by the simple model. The results presented by Rao were used to support their theory that a non-thermal noise source operates in the channel at high frequencies. Figure 6 illustrates that $|c|$ does theoretically increase with N_a, since $\overline{i_d^2}$ does not vary appreciably with substrate doping. While it is true that R_{ns} increases, the saturation drain voltage V_p and thus g_{ms} decrease with doping, so that $\overline{i_d^2} = 4kTR_{ns}g_{ms}^2$ does not vary appreciably over a wide range of substrate impurity concentrations. This is illustrated in Fig. 7, and supported by Klassen and Prins[8].

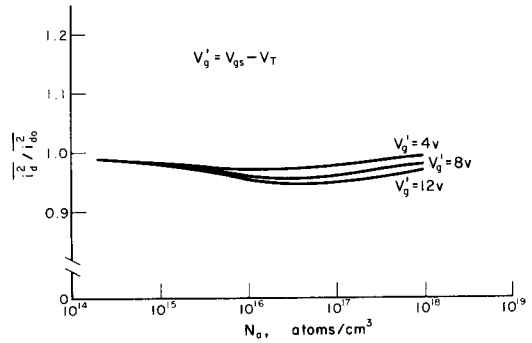

Fig. 7. Drain noise as a function of substrate doping at pinch-off, normalized to results obtained with $\phi_F = 0$.

It has recently been shown[9] that the "excess noise" does not exist, and that the observations can be attributed to measurements at insufficiently high frequencies to ensure that thermal noise is dominant.

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