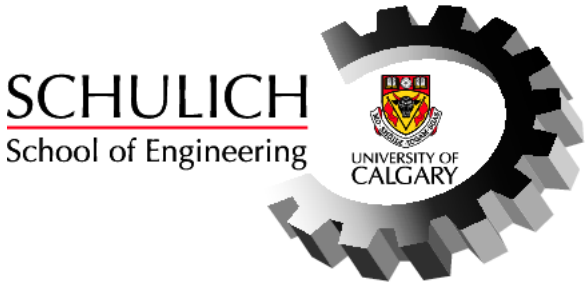

DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING

ENEL 353 - Digital Circuits

Final Examination

Wednesday, December 13, 2006
Auxiliary Gymnasium, 3:30 PM - 6:30 PM

L01 - Norm Bartley
L02 - Svetlana Yanushkevich

Instructions:

- Time allowed is 3 hours.
- The examination is closed-book.
- Non-programmable calculators are permitted.
- The maximum number of marks is 100, as indicated. Please attempt all questions.
- Please use a pen or heavy pencil to ensure legibility.
- If you use more than one examination booklet, please make sure that your name and ID number are on each.
- Where appropriate, marks will be awarded for proper and well-reasoned explanations.

Note: *Where appropriate in all of the questions below, you may assume that the system variables are available in both complemented and uncomplemented form.*

---

1. **[12 marks total.]**

   Consider the two circuits shown below in Fig. 1.

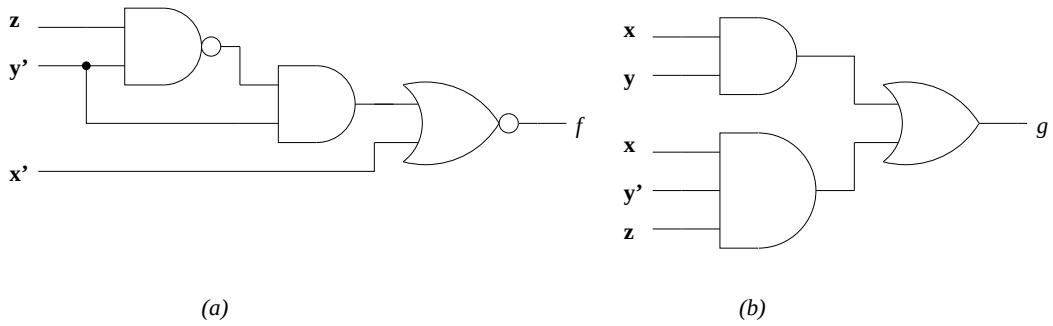

Fig. 1. Two circuits

   (a) **[4 marks]** Use algebraic transformations to prove or disprove that the two circuits given above implement the same function (do not use a truth table or Karnaugh map).

   (b) **[4 marks.]** Re-design the circuit in Fig. 1(a) using 2-input AND and XOR gates only (inverters are not available).

   (c) **[4 marks.]** Re-design the circuit in Fig. 1(b) using 2-input NAND gates only (inverters are not available).

2. **[28 marks total.]** Consider the following two functions of the four variables a, b, c, d:

$$f = \sum m(0, 4, 5, 10, 11, 13, 15)$$
$$g' = \sum m(1, 2, 12, 14)$$

   (Note that g is complemented.)

   (a) **[6 marks]** Draw Karnaugh maps and find minimal SOP and POS forms for each function.

   (b) **[6 marks.]** Implement both functions using a PLA. Try to come up with the simplest-possible solution.

(c) **[4 marks.]** Implement both functions using a ROM.

(d) **[6 marks.]** Design the circuit for the function f using 2-to-4 decoders and any additional combinational gates that you may need. The decoders have enable inputs.

(e) **[6 marks.]** Design the circuit for the function g using 2-to-1 multiplexers. No other combinational gates are available.

3. **[18 marks total.]** Consider the circuit shown below in Fig. 2.

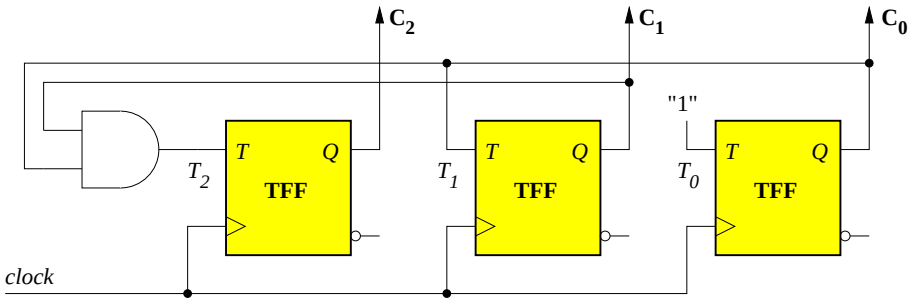

Fig. 2. Analyze and redesign this circuit

(a) **[8 marks.]** Derive the state table and the state diagram for this circuit and determine the type of the machine (Mealy or Moore). The outputs of the systems are C_2, C_1, C_0 (treat C_2 as the most-significant bit).

(b) **[2 marks.]** Based on your answer to part (a), what does this circuit implement?

(c) **[8 marks.]** Use a method of your choosing to redesign this system using JK flip-flops, and sketch the resulting circuit.

4. **[24 marks total.]** Design a 4-bit synchronous binary-coded decimal (BCD) counter using T flip-flops. The outputs are the state variables representing the count, plus an additional output Y that indicates that the count has reached "1001".

(a) **[6 marks.]** Derive the state diagram for a Moore-type system.

(b) **[6 marks.]** Create the state table that defines the current-states, next-states, TFF inputs (i.e., the excitation inputs) and the output Y.

(c) **[6 marks.]** Derive the TFF excitation equations and the output equations (use don't-cares for minimization).

(d) **[6 marks.]** Redesign the system using D flip-flops. Give the excitation and output equations for the DFF design *(it not necessary to draw the circuit).*

5. **[28 marks total.]** Design a sequential circuit using D-flip flops for a simple candy machine controller. The candy machine must release a candy after 15 cents are deposited. It has a single coin slot for dimes and nickels. It gives no change. The circuit must have two inputs (N for "nickel is deposited" and D for "dime is deposited"), and one output $OPEN$ (1 for "release a candy" and 0 for "closed").

   - Two coins cannot be inserted simultaneously.
   - You may assume that the N and D signals are produced by the sensor in such a way that they are asserted (i.e., become 1) for a very short duration that includes just one active clock edge. That is, a single coin can only cause one state transition.

   (Hint: You can do this with as few as four states!)

   (a) **[12 marks.]** Derive the state diagram for a Moore-type system. Use whatever you determine in this step for parts (b) and (c). *(Note: If you are unable to come up with a suitable solution for this part, give a state diagram for any reasonable four-state two-input system to complete parts (b) and (c).)*

   (b) **[8 marks.]** Assign the necessary number of bits (for example, using variable names Q_1 and Q_0) to represent the states of the system. Create the state table that defines the two input variables N, D, the current-states, next-states, and the output $OPEN$. Use don't-cares where appropriate.

   (c) **[8 marks.]** Implement the system using D flip-flops and whatever combinational gates you may need, and sketch the circuit.

Svetlana Yanushkevich and Norm Bartley, December 8, 2006