Name: Solutions (revised) *Lecture Section:* _____

ID#: _____

SCHULICH School of Engineering

UNIVERSITY OF CALGARY

DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING

ENEL 353 - Digital Circuits

Final Examination

Lecture sections
01: N. R. Bartley, MWF 11:00–11:50
02: S. A. Norman, MWF 12:00–12:50

Monday, December 16, 2013
Time: Noon – 3:00 PM
Location: Gold Gymnasium

Instructions:

- Time allowed is 3 hours.
- Please review the examination rules on Page 2.
- Non-programmable calculators are permitted.
- The maximum number of marks is 100, as indicated. The final examination counts toward 50% of the final grade. Please attempt all questions.
- Please use a pen or heavy pencil to ensure legibility.
- Please answer questions in the spaces provided; if space is insufficient, please use the back of the pages.
- Where appropriate, marks will be awarded for proper and well-reasoned explanations.

(Please do not write in this space.)

1 *(14)*	**2** *(14)*	**3** *(13)*	**4** *(12)*	**5** *(11)*	**6** *(10)*	**7** *(12)*	**8** *(14)*	**Total** *(100)*

Student Identification

Each candidate must sign the Seating List confirming presence at the examination. All candidates for final examinations are required to place their University of Calgary I.D. cards on their desks for the duration of the examination. (Students writing mid-term tests can also be asked to provide identity proof.) Students without an I.D. card who can produce an **acceptable** alternative I.D., e.g., one with a printed name and photograph, are allowed to write the examination.

A student without acceptable I.D. will be required to complete an Identification Form. The form indicates that there is no guarantee that the examination paper will be graded if any discrepancies in identification are discovered after verification with the student's file. **A student who refuses to produce identification or who refuses to complete and sign the Identification Form is not permitted to write the examination.**

Examination Rules

(1) Students late in arriving will not normally be admitted after one-half hour of the examination time has passed.

(2) No candidate will be permitted to leave the examination room until one-half hour has elapsed after the opening of the examination, nor during the last 15 minutes of the examination. All candidates remaining during the last 15 minutes of the examination period must remain at their desks until their papers have been collected by an invigilator.

(3) All inquiries and requests must be addressed to supervisors only.

(4) **The following is strictly prohibited:**

   (a) speaking to other candidates or communicating with them under any circumstances whatsoever;
   (b) bringing into the examination room any textbook, notebook or document not authorized by the examiner;
   (c) making use of calculators, cameras, cell-phones, computers, headsets, pagers, PDA's, or any device not authorized by the examiner;
   (d) leaving examination papers exposed to view;
   (e) attempting to read other student's examination papers.

   The penalty for violation of these rules is suspension or expulsion or such other penalty as may be determined.

(5) Candidates are requested to write on both sides of the page, unless the examiner has asked that the left hand page be reserved for rough drafts or calculations.

(6) Discarded matter is to be struck out and not removed by mutilation of the examination answer book.

(7) Candidates are cautioned against writing on their examination paper any matter extraneous to the actual answering of the question set.

(8) The candidate is to write his/her name on each answer book as directed and is to number each book.

(9) During the examination a candidate must report to a supervisor before leaving the examination room.

(10) Candidates must stop writing when the signal is given. Answer books must be handed to the supervisor-in-charge promptly. Failure to comply with this regulation will be cause for rejection of an answer paper.

(11) If during the course of an examination a student becomes ill or receives word of a domestic affliction, the student should report at once to the supervisor, hand in the unfinished paper and request that it be cancelled. If physical and/or emotional ill health is the cause, the student must report at once to a physican/counsellor so that subsequent application for a deferred examination is supported by a completed Physician/Counsellor Statement form. Students can consult professionals at University Health Services or Counselling and Student Development Centre during normal working hours or consult their physician/counsellor in the community. **Once an examination has been handed in for marking a student cannot request that the examination be cancelled for whatever reason. Such a request will be denied. Retroactive withdrawals will also not be considered.**

1. **[14 marks total.]** *Numbers, codes and binary addition.*

   (a) **[1 mark.]** Interpreted as an *unsigned binary* integer, what decimal number does 1000101 represent?

   Unsigned: $2^6 + 2^2 + 2^0 = 64 + 4 + 1 = 69_{10}$

   (b) **[1 mark.]** Interpreted as a *sign/magnitude* integer, what decimal number does 1000101 represent?

   Sign = 1 (negative), Magnitude = 000101, number is -5_{10}

   (c) **[2 marks.]** Interpreted as a *two's complement* integer, what decimal number does 1000101 represent?

   1000101 → 0111010 + 1 = 0111011

   Negative number. Determine its magnitude

   Number is $-(2^5 + 2^4 + 2^3 + 2^1 + 2^0) = -59_{10}$

   (d) **[3 marks.]** Convert the *octal* number 6572_8 to each of the formats given below. Show how you obtained your answers.

   hexadecimal: Regroup bits

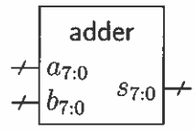
   110 101 111 010

   D 7 A $= D7A_{16}$

   decimal: $6\times8^3 + 5\times8^2 + 7\times8^1 + 2\times8^0 = 3450_{10}$

   (e) **[1 mark.]** The ten-bit Gray code for 353_{10} is 0111010001. Explain briefly but precisely why it cannot possibly be true that 0111010100 is the ten-bit Gray code for 354_{10}. Gray code ensures that an increase by 1 in the binary code causes only 1 bit to change in the Gray code. 2 bits change here.

   (f) **[2 marks.]** An example 8-bit adder is shown to the right. Recall that *signed overflow* is a condition that may occur when using an N-bit adder to add two's-complement integers.

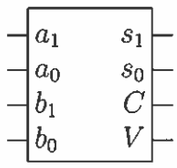
   

   Write an SOP expression involving bits of a, b, and s that is true if and only if signed overflow has occurred, and write a one-sentence explanation of why your expression is correct. (Do *not* include carry signals in your expression.)

   $V = a_7 b_7 \overline{s_7} + \overline{a_7}\,\overline{b_7} s_7$ sign bits a_7, b_7, s_7

   This will be true if adding two numbers of the same sign produces a sum with the opposite sign.

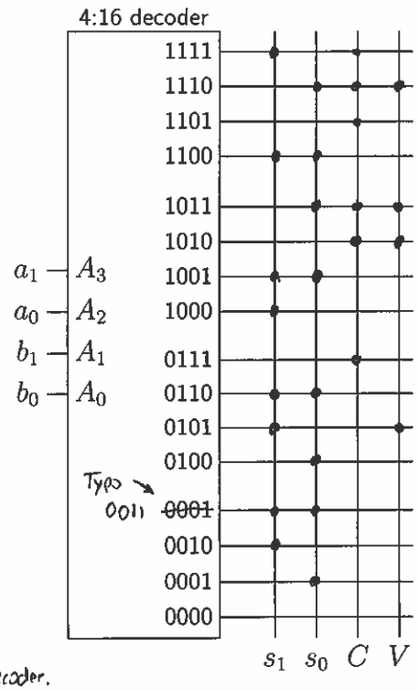
   (g) **[4 marks.]** Consider building a 2-bit integer adder, with inputs and outputs as shown to the right. $s_{1:0}$ is the 2-bit sum of $a_{1:0}$ and $b_{1:0}$, C is true to indicate unsigned overflow, and V is true to indicate signed overflow.

   Use dot notation on the given ROM circuit to show how to implement the adder as a ROM. (Hint: The given truth table will be very helpful.)

a_1	a_0	b_1	b_0	Cout	s_1	s_0	C	V
0	0	0	0	0	0	0	0	0
0	0	0	1	0	0	1	0	0
0	0	1	0	0	1	0	0	0
0	0	1	1	0	1	1	0	0
0	1	0	0	0	0	1	0	0
0	1	0	1	0	1	0	0	1
0	1	1	0	0	1	1	0	0
0	1	1	1	1	0	0	1	0
1	0	0	0	0	1	0	0	0
1	0	0	1	0	1	1	0	0
1	0	1	0	1	0	0	1	1
1	0	1	1	1	0	1	1	1
1	1	0	0	0	1	1	0	0
1	1	0	1	1	0	0	1	0
1	1	1	0	1	0	1	1	1
1	1	1	1	1	1	0	1	0

Note reverse order of input combinations between table and decoder.



2. [**14 marks total.**] *Boolean algebra and multiplexers.*

(a) [**2 marks.**] The XOR operator has a number of its own important basic properties. In the table below, determine the result of each XOR operation.

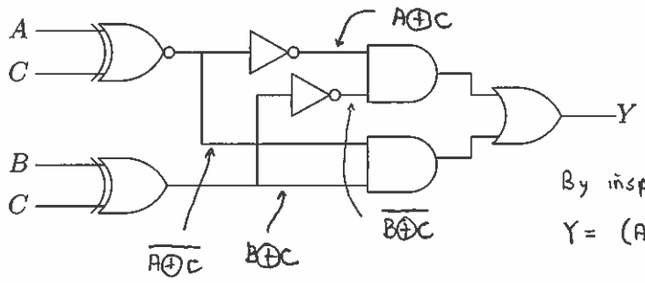
Operation	Result
$A \oplus A$	0
$A \oplus 1$	$\bar{A}$
$A \oplus \bar{B}$	$\overline{A \oplus B}$

$A \oplus A = A\bar{A} + \bar{A}A = 0$

$A \oplus 1 = A \cdot 0 + \bar{A} \cdot 1 = \bar{A}$

$A \oplus \bar{B} = AB + \bar{A}\bar{B} = \overline{A \oplus B}$

(b) [**5 marks.**] In the circuit shown below, *algebraically* prove or disprove that $Y = A \oplus B$. Do not use a truth table or K-map.



By inspection,

$Y = (A \oplus C)\overline{(B \oplus C)} + \overline{(A \oplus C)}(B \oplus C)$

Let $W = A \oplus C$, $X = B \oplus C$

Then, $Y = W\bar{X} + \bar{W}X = W \oplus X$

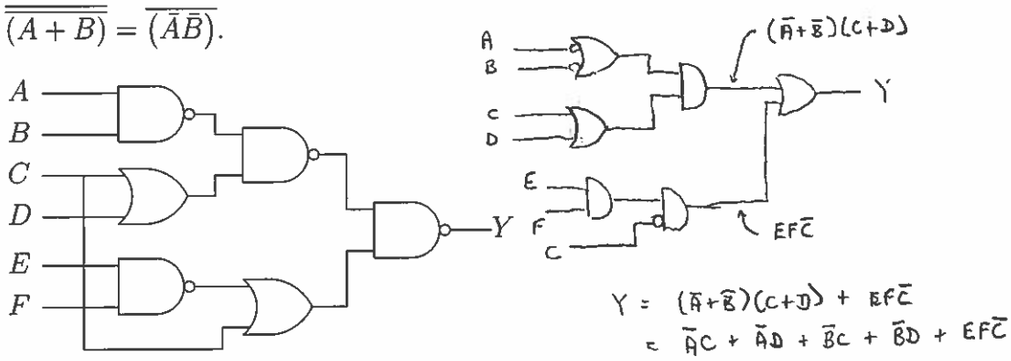
Therefore, $Y = A \oplus C \oplus B \oplus C$

$= A \oplus B \oplus C \oplus C$

from part (a), $C \oplus C = 0$

$Y = A \oplus B$

(c) [**3 marks.**] Use bubble-pushing and/or algebra to find a SOP expression for Y. If you use bubble-pushing, draw your equivalent circuit to the right of the given circuit. Hint for bubble-pushing with OR gates: $A + B = \overline{\overline{(A+B)}} = \overline{(\bar{A}\bar{B})}$.



$Y = (\bar{A}+\bar{B})(C+D) + EF\bar{C}$

$= \bar{A}C + \bar{A}D + \bar{B}C + \bar{B}D + EF\bar{C}$

(d) [**4 marks.**] Draw a schematic to show how the function $Y = AB + \bar{B}C + A\bar{C}$ can be implemented with a 2:1 multiplexer, *one* inverter, and *one* two-input AND gate.

Truth table

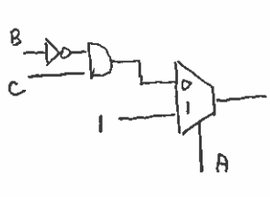
A B C	Y
0 0 0	0
0 0 1	1
0 1 0	0
0 1 1	0
1 0 0	1
1 0 1	1
1 1 0	1
1 1 1	1

⇒

A B	Y
0 0	C
0 1	0
1 0	1
1 1	1

⇒

A	Y
0	BC
1	1



3. **[13 marks total.]** *K-map and multiple-output problems.*

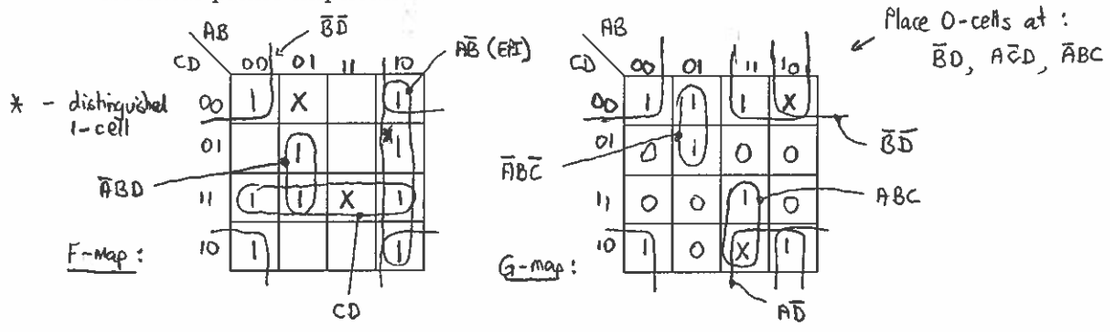
(a) **[6 marks.]** Consider the following two logic functions with the given don't-care conditions:

Function	Expression	Don't-cares
$F(A,B,C,D)$	$\bar{B}\bar{C}\bar{D} + A\bar{B} + \bar{A}\bar{B}C + \bar{A}BD$	$\bar{A}B\bar{C}\bar{D}$, $ABCD$
$G(A,B,C,D)$	$(B+\bar{D})(\bar{A}+C+\bar{D})(A+\bar{B}+\bar{C})$	$A\bar{B}\bar{C}\bar{D}$, $ABC\bar{D}$

Use the blank K-maps below to determine minimal SOP expressions for each of F and G:

i. If there is more than one solution for either, give just one, but indicate how many other solutions are possible;

ii. On the map for F, indicate all of the distinguished 1-cells and the essential prime implicants.



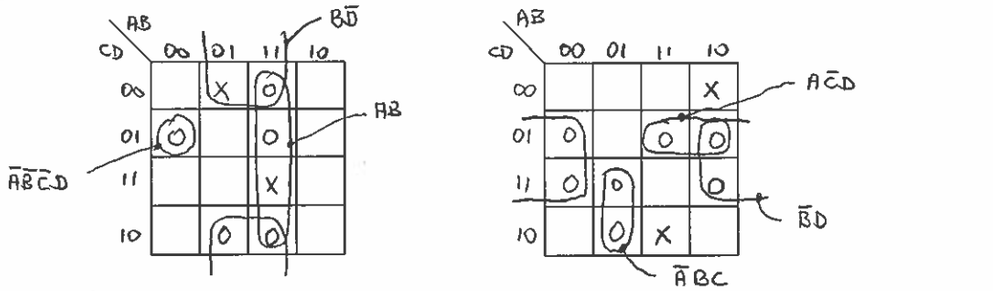
$F = \bar{B}\bar{D} + A\bar{B} + CD + \bar{A}BD$

There are two other possible solutions

$G = \bar{B}\bar{D} + ABC + A\bar{D} + \bar{A}B\bar{C}$

There is one other possible solution

(b) **[4 marks.]** Use the same maps from part (a) to determine minimal POS expressions for each of F and G. If there are multiple solutions, give just one.



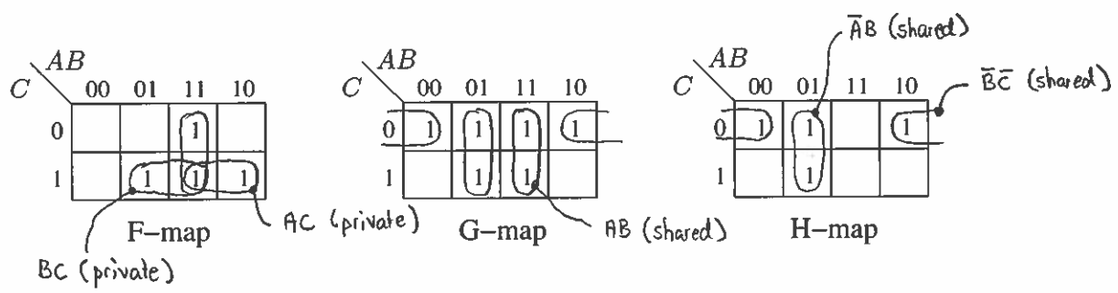
$\bar{F} = \bar{B}\bar{D} + AB + \bar{A}\bar{B}\bar{C}D$

so $F = (\bar{B}+D)(\bar{A}+\bar{B})(A+B+C+\bar{D})$

$\bar{G} = \bar{A}BC + \bar{B}D + A\bar{C}D$

so $G = (A+\bar{B}+\bar{C})(B+\bar{D})(\bar{A}+C+\bar{D})$

(c) **[3 marks.]** The K-maps below describe a system with three inputs and three outputs. Write equations for F, G, and H suitable for implementation on a PLA using the *smallest number of implicants*. Do not draw a PLA diagram.

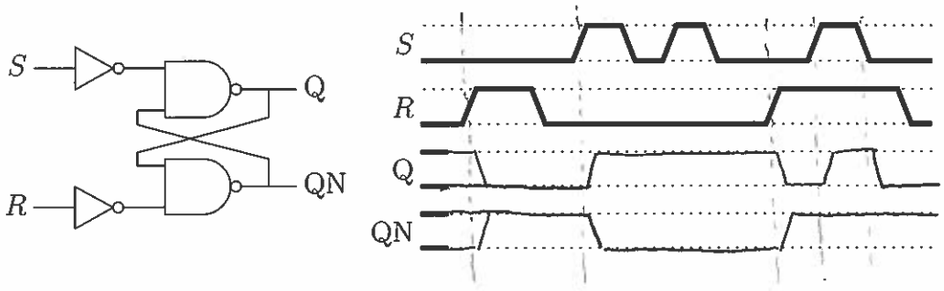


$F = \bar{A}B + BC + AC$ $G = \bar{A}B + AB + \bar{B}\bar{C}$ $H = \bar{A}B + \bar{B}\bar{C}$

There are a total of 5 implicants used (3 shared, 2 private).

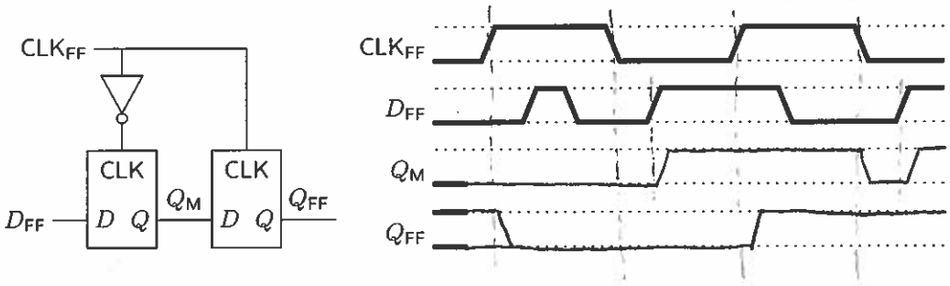
4. **[12 marks total.]** *Questions about basic building blocks for sequential circuits.*

(a) **[3 marks.]** An SR latch can be made from two NOT gates and two NAND gates, as shown below. Complete the timing diagram. (Note that for the given S and R signals, it's possible to determine Q and QN at all times.)



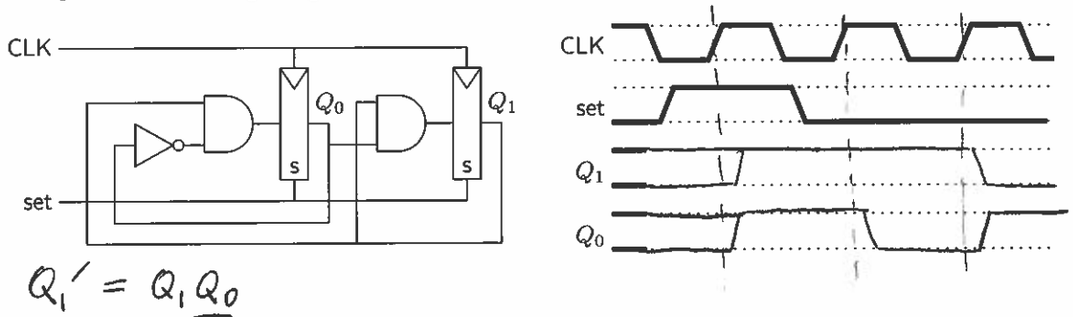
Remark: When S=R=1, both NAND gates have a 0 input, so Q=QN=1.

(b) **[3 marks.]** The schematic below shows a D flip-flop made from two D latches in a master-slave configuration. Complete the timing diagram.



Remark: Because of the NOT gate, Q_M follows D_{FF} when CLK_{FF} is LOW.

(c) **[3 marks.]** The *set* inputs to the DFFs in this circuit are *synchronous*. Complete the timing diagram.

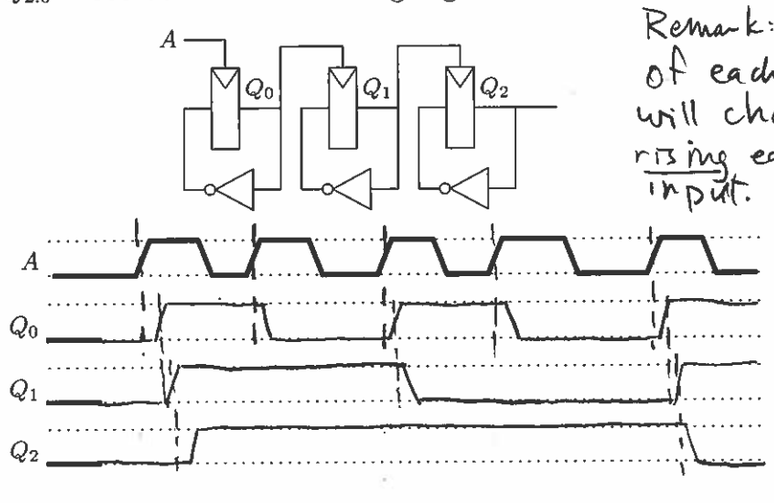


$Q_1' = Q_1 Q_0$

$Q_0' = Q_1 \overline{Q_0}$

(d) **[3 marks.]** Usually all the D flip-flops in a sequential logic circuit are connected to the same clock source. However, it's possible to create some interesting and useful circuits by breaking that rule.

Complete the timing diagram for the given circuit. Assume that the pulses on A are much wider than any of the DFF timing parameters, and that $Q_{2:0} = 000$ before the first rising edge on A.



Remark: The output of each flip-flop will change on each rising edge of its clock input.

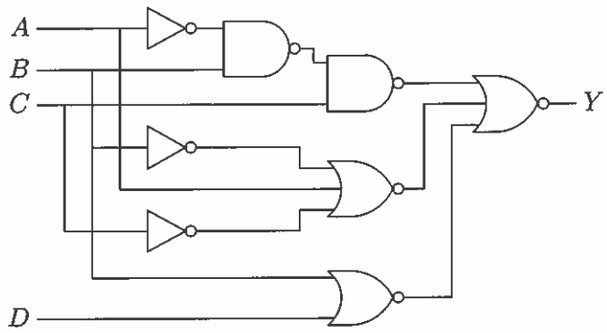
5. **[11 marks total.]** *Constraints related to voltage levels and timing.*

(a) **[3 marks.]** The table below on the left specifies important voltage levels for Advanced Ultra-Low Voltage CMOS operating with $V_{DD} = 1.8\,V$. Fill in the table on the right with either the most precise possible range of output voltages, or an explanation of why the range is unknown.

V_{OH}	1.20 V
V_{IH}	1.17 V
V_{IL}	0.63 V
V_{OL}	0.45 V

gate	output range or explanation	Remarks
1.18 V →	$0 \le V_{out} \le 0.45V$	$V_{in} \ge V_{IH}$
0.05 V, 0.50 V, 1.05 V →	Unknown. Two inputs are OK, but 1.05V is in forbidden zone	
0.52 V, 1.70 V →	$1.20V \le V_{out} \le 1.8V$	$0.52V \le V_{IL}$, $1.70V \ge V_{IH}$

(b) **[3 marks.]** Determine overall t_{pd} and t_{cd} values for the following circuit. Show carefully how you obtained your answers.



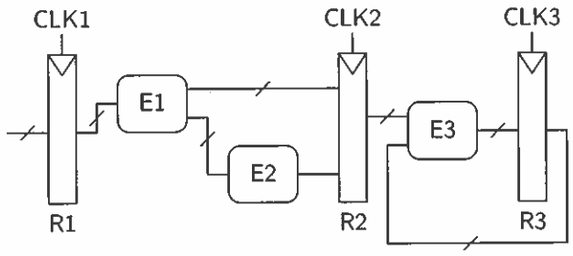
Timing parameters in ps

gate	# inputs	t_{pd}	t_{cd}
NOT	1	30	21
NAND	2	43	32
NAND	3	53	42
NOR	2	55	40
NOR	3	70	54

overall $t_{pd} = \underbrace{30}_{\text{NOT}} + \underbrace{43}_{\text{NAND2}} + \underbrace{43}_{\text{NAND2}} + \underbrace{70}_{\text{NOR3}} = \boxed{186\,ps}$

overall $t_{cd} = \underbrace{32}_{\text{NAND2}} + \underbrace{54}_{\text{NOR3}} = \boxed{86\,ps}$

(c) **[2 marks.]** In the following circuit, signals CLK1, CLK2, and CLK3 all come from the same clock source. For all three registers, the timing parameters are $t_{setup} = 50\,ps$, $t_{hold} = 0\,ps$, $t_{pcq} = 40\,ps$, and $t_{ccq} = 25\,ps$.



Timing parameters in ps

element	t_{pd}	t_{cd}
E1	100	41
E2	200	55
E3	280	70

Assume the input to R1 never violates timing constraints, and that there is zero clock skew between CLK1, CLK2, and CLK3. Determine the minimum T_C (clock period) for reliable operation of the circuit.

The critical path is from R1 to R2 thru E1 and E2.

$t_{pd} = 100 + 200 = 300\,ps.$

$T_c \le t_{pcq} + t_{pd} + t_{setup} = 40 + 300 + 50 = \boxed{390\,ps}$

(d) **[3 marks.]** Consider again the circuit of part (c), but now assume that there might be some clock skew. Suppose the desired T_C is 460 ps. What is the maximum value of t_{skew} that will allow reliable operation?

Setup: From (c), $t_{pd} = 300ps$

$t_{skew} \le T_c - t_{pcq} - t_{pd} - t_{setup}$

$\le 460 - 40 - 300 - 50$

$t_{skew} \le 70\,ps$

Hold: Overall t_{cd} is 41ps (R1 to R2 thru E1)

$t_{cd} \ge t_{hold} - t_{ccq} + t_{skew}$

$t_{skew} \le t_{cd} - t_{hold} + t_{ccq} = 41 - 0 + 25$

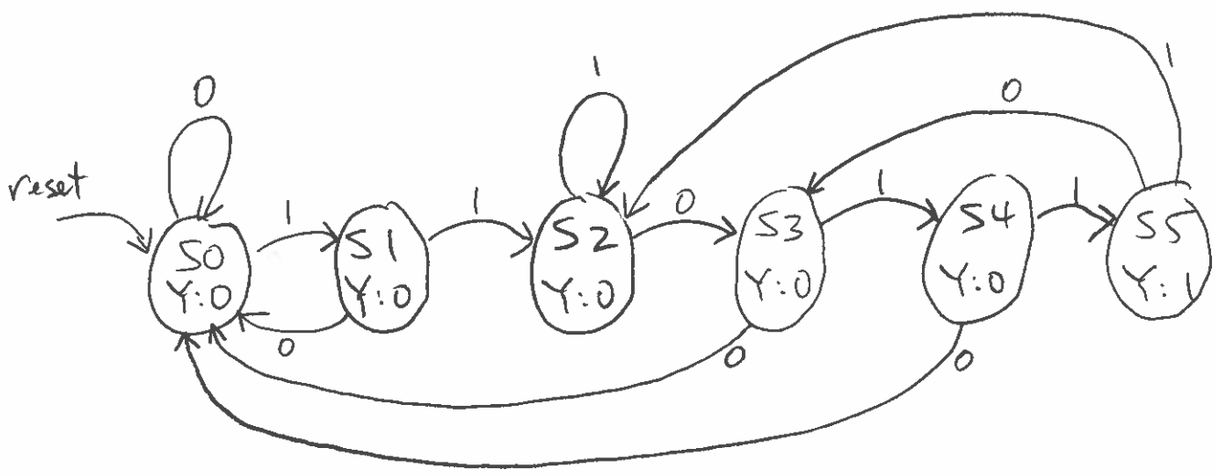
$t_{skew} \le 66\,ps$

Overall: $\boxed{t_{skew} \le 66\,ps}$

6. **[10 marks total.]** *A sequence detection problem.* Consider the design of a Moore-type FSM that has one input A and one output Y. Y should be 1 if the values of A at the last 5 rising edges of the clock have been 1, 1, 0, 1, 1. Y should be 0 at all other times.

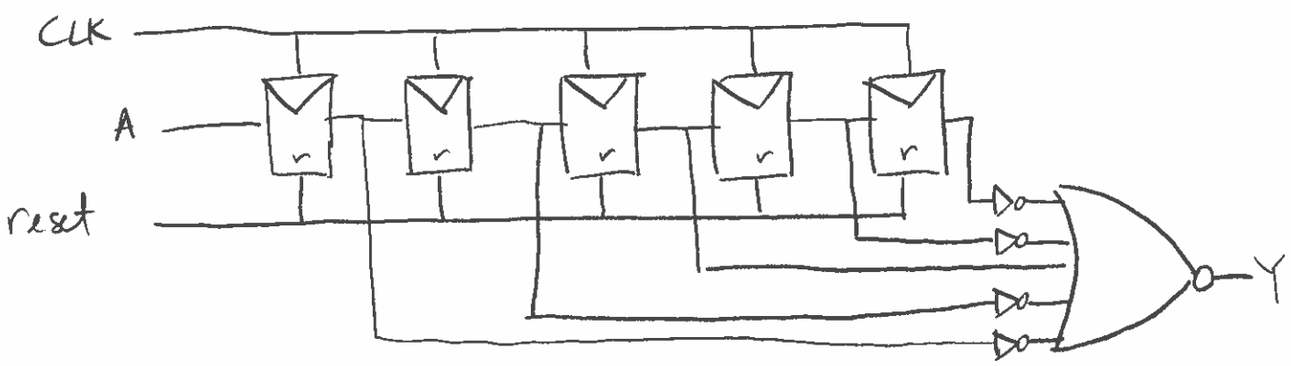
   (a) **[7 marks.]** Choose states for an FSM design, and describe them in the table below. (If you need fewer than eight states, write "unused" beside the names of states you don't use.) Then make a **state-transition diagram** for the FSM.

state	description
S0	*from reset, or looking for first 1 in 11011*
S1	looking for second 1 in 11011
S2	looking for 0 within 11011
S3	looking for third 1 in 11011
S4	looking for fourth 1 in 11011
S5	sequence detected over last 5 rising edges
S6	unused
S7	unused



Remark: The direct path from S0 to S5 is easy. The harder part is determining how far to "back up" when an "undesired bit" arrives.

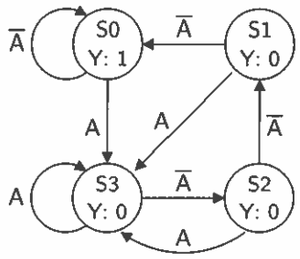
   (b) **[3 marks.]** Instead of going on to make tables for next-state and output logic, consider a totally different method of implementation. Draw a schematic for the sequence detector, using 5 D flip-flops in a shift register configuration, one NOR gate with however many inputs you need, and some inverters.



Remark: Remember that DeMorgan's Theorem lets you convert a NOR gate into an AND gate.

7. **[12 marks total.]** *FSM implementation in a "programmable FSM" circuit.*

(a) **[4 marks.]** Below are a state transition diagram of an FSM and a proposed state encoding. Write truth tables for the next-state and output logic.



state	S_1	S_0
S0	0	0
S1	0	1
S2	1	0
S3	1	1

next-state logic

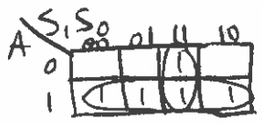
S_1	S_0	A	S_1'	S_0'
0	0	0	0	0
0	0	1	1	1
0	1	0	0	0
0	1	1	1	1
1	0	0	0	1
1	0	1	1	1
1	1	0	1	0
1	1	1	1	1

output logic

S_1	S_0	Y
0	0	1
0	1	0
1	0	0
1	1	0

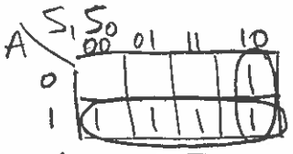
(b) **[3 marks.]** Use the results of part (a) to find minimal SOP expressions for the next-state and output logic.

S_1'



$S_1' = S_1 S_0 + A$

S_0'



$S_0' = S_1 \overline{S_0} + A$

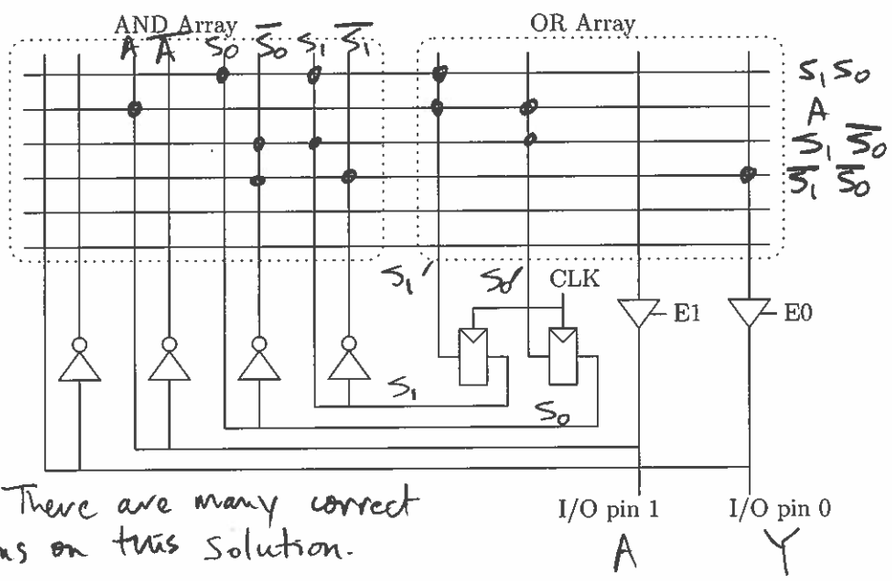
By inspection

$Y = \overline{S_1}\,\overline{S_0}$

(c) **[5 marks.]** The FSM can be implemented using a "programmable FSM", which combines a PLA, some D flip-flops, and some tristate buffers, as shown below. A decision has been made to use I/O pin 1 for A and I/O pin 0 for Y.

Fill in the table to specify and explain the correct values for E1 and E0, then put dots in the AND and OR Arrays in the PLA to implement your equations from part (b).

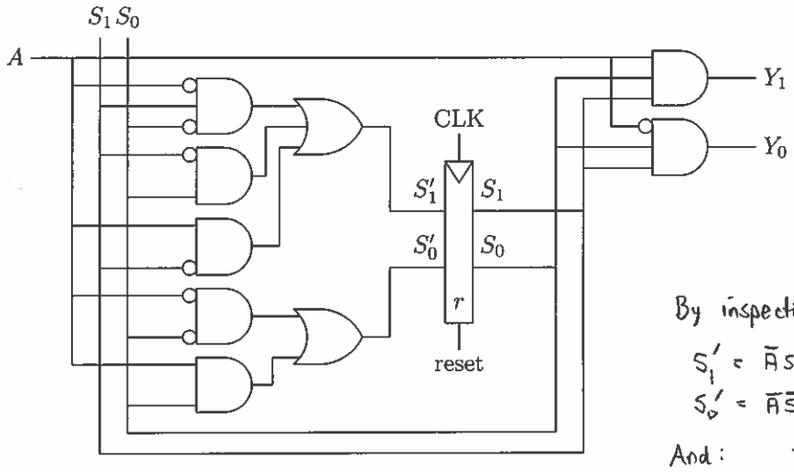
signal	0 or 1?	reason
E1	0	A must not contend with OR array output.
E0	1	Y must be driven by OR array output.



Remark: There are many correct variations on this solution.

8. **[14 marks total.]** *Questions about FSM analysis.*

(a) **[8 marks.]** Consider the FSM sketched below. There is one input A, and two outputs Y_1 and Y_0. Determine the combined state and output table, and sketch the state-transition diagram. In your tables, use 0's and 1's for the states and next states, not symbols like S0, S1, etc.



By inspection:

$S_1' = \bar{A} S_1 \bar{S}_0 + \bar{S}_1 S_0 + A \bar{S}_1$

$S_0' = \bar{A} \bar{S}_0 + A S_0$

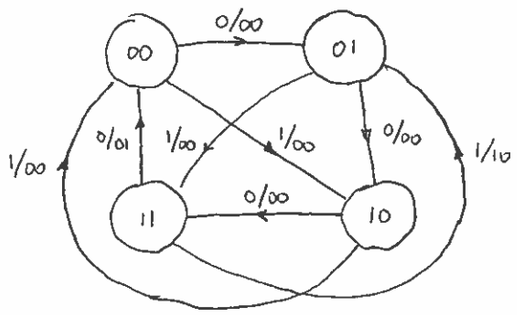
And: $Y_1 = A S_1 S_0$

$Y_0 = \bar{A} S_1 S_0$

Combined state and output table:

Current state $S_1 S_0$	input A	next-state $S_1' S_0'$	output $Y_1 Y_0$
00	0	01	00
00	1	10	00
01	0	10	00
01	1	11	00
10	0	11	00
10	1	00	00
11	0	00	01
11	1	01	10

State-transition diagram:



(b) **[6 marks.]** Below is the combined state and output table for a FSM that has one input A, and one output Y. The state variables are $S_{2:0}$. Use this table to complete the timing diagram.

$S_{2:0}$	A	$S'_{2:0}$	Y	$S_{2:0}$	A	$S'_{2:0}$	Y
000	0	000	0	010	1	010	0
000	1	001	0	011	0	100	0
001	0	000	0	011	1	001	0
001	1	010	0	100	0	000	0
010	0	011	0	100	1	010	1