Name: _____ *Lecture Section:* _____

ID#: _____

SCHULICH School of Engineering

UNIVERSITY OF CALGARY

DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING

ENEL 353 - Digital Circuits

Final Examination

Lecture sections
01: N. R. Bartley, MWF 11:00–11:50, ENC 241
02: S. A. Norman, MWF 11:00–11:50, ST 145

Wednesday, December 17, 2014
Time: 7:00 PM – 10:00 PM
Locations: ICT 102 for section 01, EDC 179 for section 02

Instructions:

- Time allowed is 3 hours.
- Please review the examination rules on Page 2.
- Non-programmable calculators are permitted.
- The maximum number of marks is 98, as indicated. The final examination counts toward 50% of the final grade. Please attempt all questions.
- Please use a pen or heavy pencil to ensure legibility.
- Please answer questions in the spaces provided; if space is insufficient, please use the back of the pages.
- Where appropriate, marks will be awarded for proper and well-reasoned explanations.

(Please do not write in this space.)

1 *(15)*	**2** *(14)*	**3** *(12)*	**4** *(12)*	**5** *(10)*	**6** *(11)*	**7** *(10)*	**8** *(14)*	**Total** *(98)*

Student Identification

Each candidate must sign the Seating List confirming presence at the examination. All candidates for final examinations are required to place their University of Calgary I.D. cards on their desks for the duration of the examination. (Students writing mid-term tests can also be asked to provide identity proof.) Students without an I.D. card who can produce an **acceptable** alternative I.D., e.g., one with a printed name and photograph, are allowed to write the examination.

A student without acceptable I.D. will be required to complete an Identification Form. The form indicates that there is no guarantee that the examination paper will be graded if any discrepancies in identification are discovered after verification with the student's file. **A student who refuses to produce identification or who refuses to complete and sign the Identification Form is not permitted to write the examination.**

Examination Rules

(1) Students late in arriving will not normally be admitted after one-half hour of the examination time has passed.

(2) No candidate will be permitted to leave the examination room until one-half hour has elapsed after the opening of the examination, nor during the last 15 minutes of the examination. All candidates remaining during the last 15 minutes of the examination period must remain at their desks until their papers have been collected by an invigilator.

(3) All inquiries and requests must be addressed to supervisors only.

(4) **The following is strictly prohibited:**

   (a) speaking to other candidates or communicating with them under any circumstances whatsoever;
   (b) bringing into the examination room any textbook, notebook or document not authorized by the examiner;
   (c) making use of calculators, cameras, cell-phones, computers, headsets, pagers, PDA's, or any device not authorized by the examiner;
   (d) leaving examination papers exposed to view;
   (e) attempting to read other student's examination papers.

   The penalty for violation of these rules is suspension or expulsion or such other penalty as may be determined.

(5) Candidates are requested to write on both sides of the page, unless the examiner has asked that the left hand page be reserved for rough drafts or calculations.

(6) Discarded matter is to be struck out and not removed by mutilation of the examination answer book.

(7) Candidates are cautioned against writing on their examination paper any matter extraneous to the actual answering of the question set.

(8) The candidate is to write his/her name on each answer book as directed and is to number each book.

(9) During the examination a candidate must report to a supervisor before leaving the examination room.

(10) Candidates must stop writing when the signal is given. Answer books must be handed to the supervisor-in-charge promptly. Failure to comply with this regulation will be cause for rejection of an answer paper.

(11) If during the course of an examination a student becomes ill or receives word of a domestic affliction, the student should report at once to the supervisor, hand in the unfinished paper and request that it be cancelled. If physical and/or emotional ill health is the cause, the student must report at once to a physican/counsellor so that subsequent application for a deferred examination is supported by a completed Physician/Counsellor Statement form. Students can consult professionals at University Health Services or Counselling and Student Development Centre during normal working hours or consult their physician/counsellor in the community. **Once an examination has been handed in for marking a student cannot request that the examination be cancelled for whatever reason. Such a request will be denied. Retroactive withdrawals will also not be considered.**

1. **[15 marks total.]** *Numbers, codes and binary addition.*

   (a) **[3 marks.]** Convert the fourteen-bit unsigned binary number 10011111011010_2 to hexadecimal and octal representations.

   hexadecimal **octal**

   (b) **[1 mark.]** One of the following bit patterns is valid BCD (binary-coded decimal), but the other one is not: 100110110100, 100100111000. Which one is not valid? *For credit to be given, you must give a correct reason.*

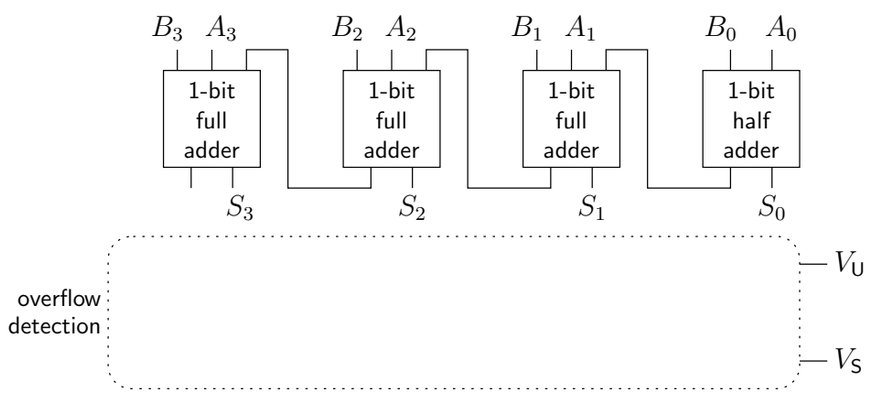
   (c) **[1 mark.]** What number does the valid bit pattern from part (b) represent? Give your answer in base ten.

   (d) **[3 marks.]** Use repeated division to find the unsigned binary representation of 53_{10}.

   (e) **[2 marks.]** Find the decimal representation of $1AB_{16}$. Show your work.

   (f) **[3 marks.]** Unlike a 1-bit full-adder, which has three inputs, a *1-bit half-adder* circuit computes the sum and carry-out of only *two* input bits. Use of a half-adder is shown in the four-bit adder of part (g) below. Draw a schematic for a half-adder circuit, using only inverters and two-input NAND gates. Use A and B as names for inputs, and S and C_{OUT} as names for outputs.

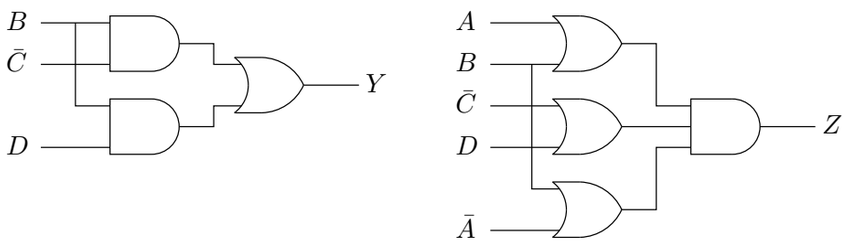
   (g) **[2 marks.]** Add wires and logic gates within the area labeled "overflow detection" so that $V_{\text{U}} = 1$ indicates unsigned overflow and $V_{\text{S}} = 1$ indicates signed overflow. You can connect your gates to whichever wires of the four-bit adder you want to use.



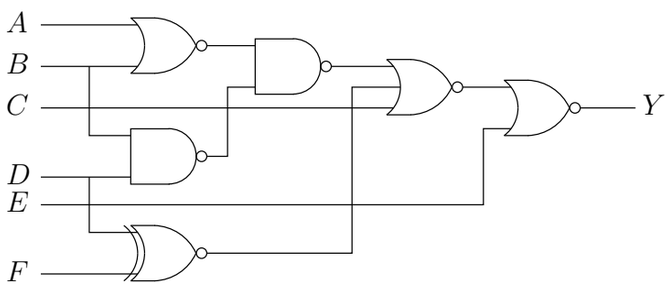
2. **[14 marks total.]** *Boolean algebra and multiplexers.*

   (a) **[4 marks.]** The *consensus theorem* in boolean algebra states that $AB + \bar{A}C = AB + \bar{A}C + BC$. *Algebraically* prove this theorem. Do not use a truth table or K-map.

   (b) **[3 marks.]** In the circuits shown below, *algebraically* prove or disprove that $Z = Y$. Do not use a truth table or K-map.



   (c) **[3 marks.]** Use bubble-pushing and/or algebra to find a SOP expression for Y. If you use bubble-pushing, draw your equivalent circuit to the right of the given circuit.



   (d) **[4 marks.]** Draw a schematic to show how the function $Y = A \oplus B \oplus C$ can be implemented with just *three* 2:1 multiplexers and *one* inverter. No other components are allowed.

3. **[12 marks total.]** *K-map problems.*

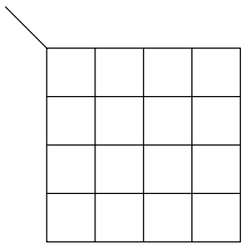
   (a) **[7 marks.]** Consider the following two logic functions given in minterm and maxterm notation with the given don't-care conditions:

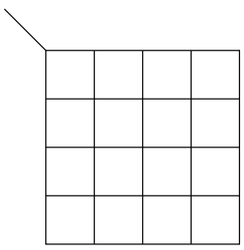
Function	**Expression**	**Don't-cares**
$F(A,B,C,D)$	$\sum(m_1, m_3, m_6, m_8, m_{11}, m_{14})$	m_{13}, m_{15}
$G(A,B,C,D)$	$\prod(M_1, M_6, M_{12}, M_{13}, M_{14})$	M_4, M_{15}

   Use the blank K-maps below to determine minimal SOP expressions for each of F and G:

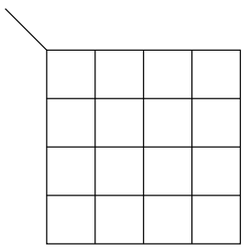
   i. If there is more than one solution for either, give just one, but indicate how many other solutions are possible;

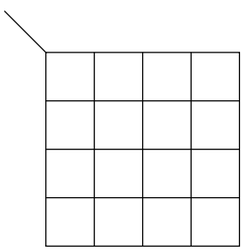
   ii. On the map for F, indicate all of the distinguished 1-cells and the essential prime implicants.





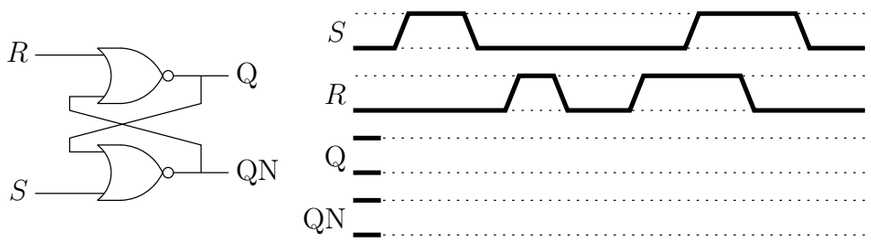
   (b) **[5 marks.]** Use the same maps from part (a) to determine minimal POS expressions for each of F and G. If there are multiple solutions, give just one.



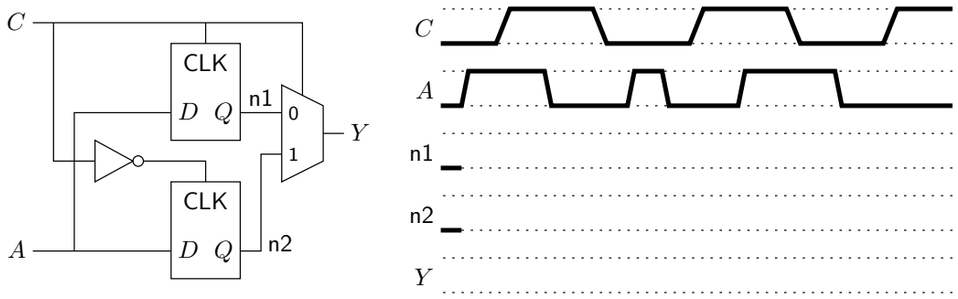


4. **[12 marks total.]** *Questions about basic building blocks for sequential circuits.*

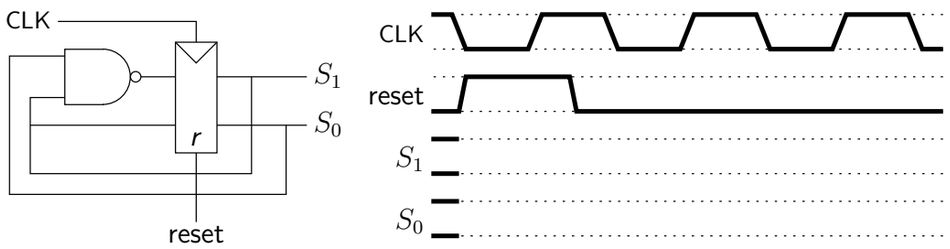
(a) **[3 marks.]** The schematic below shows an SR latch made from two NOR gates. Complete the timing diagram. (Note that for the given S and R signals, it's possible to determine Q and QN at all times.)



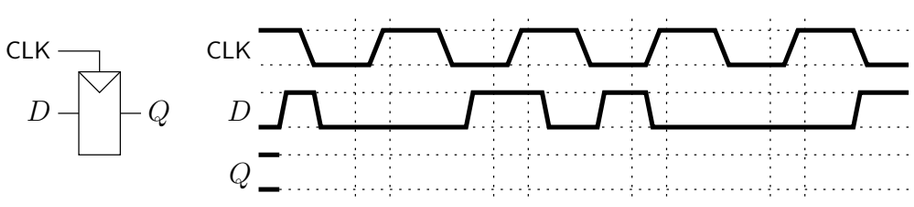
(b) **[4 marks.]** The schematic below shows a circuit built with two D latches, an inverter, and a 2:1 mux. Complete the timing diagram.



(c) **[3 marks.]** The *reset* input to the 2-bit register in this circuit is *asynchronous*. Complete the timing diagram.



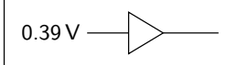
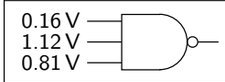
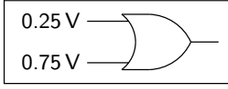
(d) **[2 marks.]** The vertical dotted lines in the timing diagram below indicate the setup-and-hold apertures around rising clock edges. Complete the timing diagram, clearly indicating any time intervals in which the DFF could be in a metastable state. Assume that for the DFF $t_{\mathrm{ccq}} > t_{\mathrm{hold}}$, and show appropriate delays on Q.



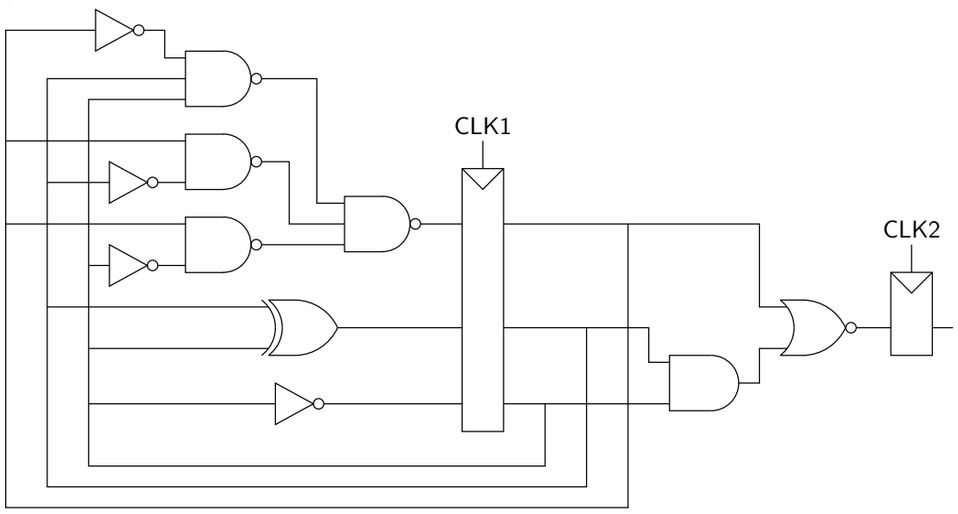
5. **[10 marks total.]** *Constraints related to voltage levels and timing.*

(a) **[3 marks.]** The table below on the left specifies important voltage levels for Advanced Ultra-Low Voltage CMOS operating with $V_{DD} = 1.2\,V$. Fill in the table on the right with either the most precise possible range of output voltages, or an explanation of why the range is unknown.

V_{OH}	0.80 V
V_{IH}	0.78 V
V_{IL}	0.42 V
V_{OL}	0.30 V

gate	output range or explanation
	
	
	

(b) **[3 marks.]**



Suppose that CLK1 and CLK2 come from the same source, and there is zero skew between them. Here are the timing parameters for both the 3-bit register and the DFF: $\mathbf{t}_{setup} = 50\,ps$, $\mathbf{t}_{hold} = 10\,ps$, $\mathbf{t}_{pcq} = 40\,ps$, and $\mathbf{t}_{ccq} = 25\,ps$. Timing parameters for logic gates, in ps, are given in the table below to the right.

What is the shortest clock period T_C allowable for reliable operation of the circuit? *Show your work.*

gate	# inputs	$\mathbf{t}_{pd}$	$\mathbf{t}_{cd}$
NOT	1	30	21
NAND	2	43	32
NAND	3	53	42
NOR	2	50	37
AND	2	55	40
XOR	2	70	54

(c) **[4 marks.]** Consider again the circuit of part (b), but now assume that there might be some clock skew. Suppose the desired T_C is 260 ps. What is the maximum value of $\mathbf{t}_{skew}$ that will allow reliable operation?

6. **[11 marks total.]** *FSM implementation in a "programmable FSM" circuit.*

An engineer has designed a Moore-type FSM. $Q_{2:0}$ is the name for the state and B is the name for the one-bit input. Next-state and output equations are:

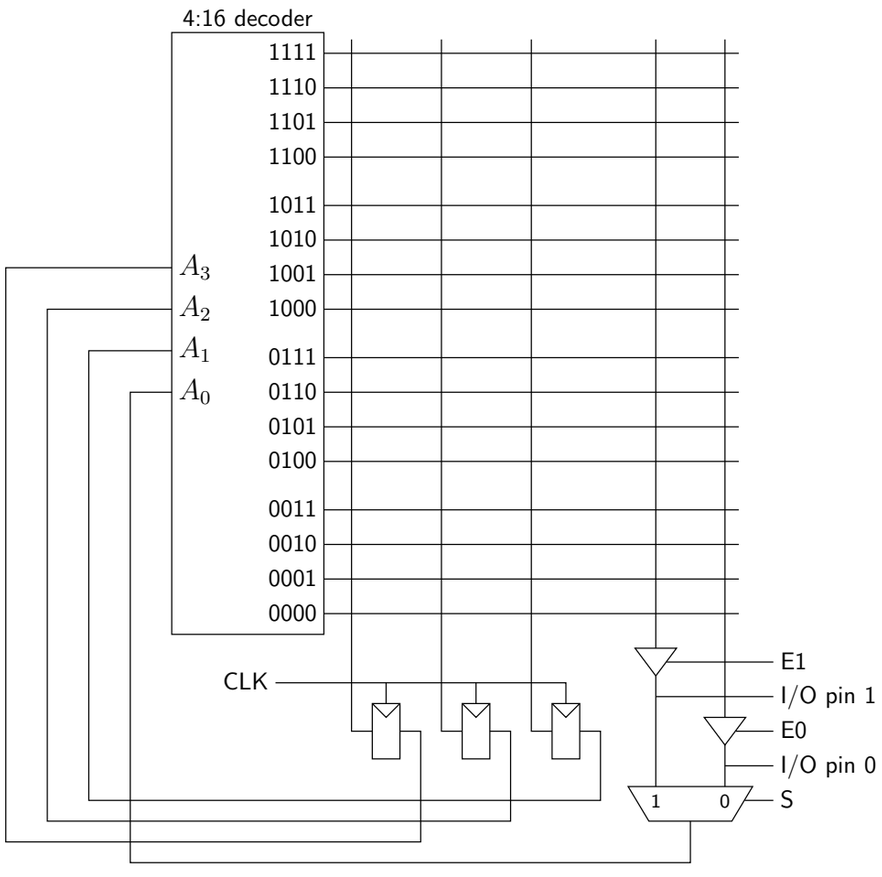
$$Q_2' = Q_2\,\overline{Q_1}\,\overline{Q_0} + Q_2\,\overline{Q_1}\,B + Q_1\,Q_0\,\overline{B}$$
$$Q_1' = Q_1\,\overline{Q_0} + \overline{Q_1}\,Q_0\,B$$
$$Q_0' = Q_1\,\overline{Q_0}\,\overline{B} + \overline{Q_1}\,\overline{Q_0}\,B + Q_1\,Q_0\,B$$
$$Y = Q_2\,Q_1\,\overline{Q_0}$$

The FSM will be implemented using a ROM array and a few other components that should be familiar to you. The circuit is shown at the bottom of the page.

(a) **[3 marks.]** A decision has been made to use I/O pin 0 for B and I/O pin 1 for Y. Fill in the table to specify and explain the correct values for the tristate enable signals E1 and E0 and the mux select signal S.

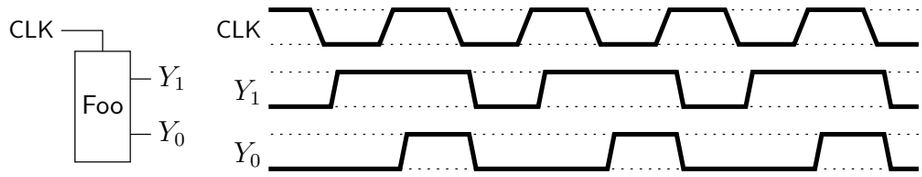
signal	**0 or 1?**	**reason**
E1		
E0		
S		

(b) **[8 marks.]** Use dot notation on the given ROM array to show how to implement the next-state and output logic for the FSM. *Use the space above and beside the schematic to show any work you need to do to decide where to place dots.*



7. **[10 marks.]** *An FSM-like system that updates twice per clock cycle.*

   Consider the device labeled Foo below, and the associated timing diagram. The two-bit signal $Y_{1:0}$ repeats the bit pattern 00, 10, 11, 00, 10, 11, ..., indefinitely.



   Implementing Foo as a Moore-type FSM would be easy if updates to $Y_{1:0}$ happened only on rising edges of CLK, but here they happen on both rising and falling edges of CLK.

   Draw a schematic for an implementation of Foo using elements selected from this list: SR latches, D latches, DFFs, inverters, any kind of two-input logic gate, 2:1 multiplexers.

   Hints: (1) On page 6 there is a circuit that could be used to do state updates every half-cycle of CLK. (2) Starting with a Moore-type state transition diagram is a reasonable approach.

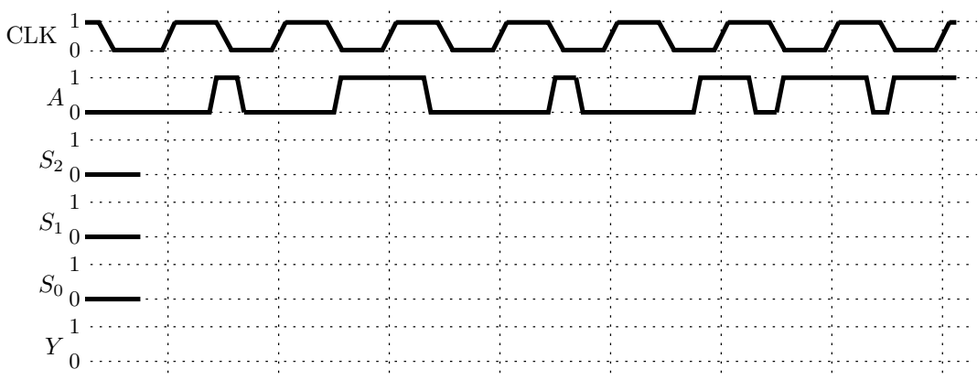
   Important: Do not start by trying to draw a schematic—show your preliminary work first.

8. **[14 marks total.]** *Questions about FSM analysis.*

(a) **[4 marks.]** Below is the combined state and output table for a Mealy-type FSM that has one input A, and one output Y. The state variables are $S_{2:0}$. Use the information in this table to sketch a state-transition diagram.

$S_{2:0}$	A	$S'_{2:0}$	Y	$S_{2:0}$	A	$S'_{2:0}$	Y
000	0	001	0	010	1	011	1
000	1	000	0	011	0	001	0
001	0	010	0	011	1	100	0
001	1	000	0	100	0	001	1
010	0	010	0	100	1	000	0

(b) **[5 marks.]** Using the table in part (a), complete the timing diagram below.



(c) **[5 marks.]** Draw a state-transition diagram for a *Moore-type* FSM that mimics the Mealy-type FSM of part (a) as closely as possible. Hypothetically, for example, if the Mealy output is 1 when the current input is 0 and the input has been 0 at the last three rising edges of CLK, then the Moore output should be 1 when the input has been 0 at the last four rising edges of CLK.