Name: Solutions

ID#: _____

Section: _____

(L01 was with N. Bartley in ENE 243; L02 was with S. Norman in ST 141.)

SCHULICH School of Engineering

UNIVERSITY OF CALGARY

DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING

ENEL 353 - Digital Circuits

Fall 2019 Final Examination

Course instructors: Norm Bartley and Steve Norman

Monday, December 9, 2019
Start Time: 7:00 PM
Location: Gold Gym

Instructions:

- Time allowed is 3 hours.
- Please review the examination rules on Page 2.
- You may use a calculator, but it must be one of the following sanctioned Schulich School of Engineering models: Casio FX-260, Casio FX-300MS, Texas Instruments TI-30XIIS.
- The maximum number of marks is 103, as indicated. The final examination counts toward 50% of the final grade. Please attempt all questions.
- Please use a pen or heavy pencil to ensure legibility.
- Please answer questions in the spaces provided; if space is insufficient, please use the back of the pages.
- Where appropriate, marks will be awarded for proper and well-reasoned explanations.

(Please do not write in this space.)

1 *(12)*	**2** *(11)*	**3** *(12)*	**4** *(12)*	**5** *(11)*	**6** *(13)*	**7** *(10)*	**8** *(12)*	**9** *(10)*	**Total** *(103)*

Student Identification

Each candidate must sign the Seating List confirming presence at the examination. All candidates for final examinations are required to place their University of Calgary I.D. cards on their desks for the duration of the examination. (Students writing mid-term tests can also be asked to provide identity proof.) Students without an I.D. card who can produce an **acceptable** alternative I.D., e.g., one with a printed name and photograph, are allowed to write the examination.

A student without acceptable I.D. will be required to complete an Identification Form. The form indicates that there is no guarantee that the examination paper will be graded if any discrepancies in identification are discovered after verification with the student's file. **A student who refuses to produce identification or who refuses to complete and sign the Identification Form is not permitted to write the examination.**

Examination Rules

(1) Students late in arriving will not normally be admitted after one-half hour of the examination time has passed.
(2) No candidate will be permitted to leave the examination room until one-half hour has elapsed after the opening of the examination, nor during the last 15 minutes of the examination. All candidates remaining during the last 15 minutes of the examination period must remain at their desks until their papers have been collected by an invigilator.
(3) All inquiries and requests must be addressed to supervisors only.
(4) **The following is strictly prohibited:**
    (a) speaking to other candidates or communicating with them under any circumstances whatsoever;
    (b) bringing into the examination room any textbook, notebook or document not authorized by the examiner;
    (c) making use of calculators, cameras, cell-phones, computers, headsets, pagers, PDA's, or any device not authorized by the examiner;
    (d) leaving examination papers exposed to view;
    (e) attempting to read other student's examination papers.

    The penalty for violation of these rules is suspension or expulsion or such other penalty as may be determined.
(5) Candidates are requested to write on both sides of the page, unless the examiner has asked that the left hand page be reserved for rough drafts or calculations.
(6) Discarded matter is to be struck out and not removed by mutilation of the examination answer book.
(7) Candidates are cautioned against writing on their examination paper any matter extraneous to the actual answering of the question set.
(8) The candidate is to write his/her name on each answer book as directed and is to number each book.
(9) During the examination a candidate must report to a supervisor before leaving the examination room.
(10) Candidates must stop writing when the signal is given. Answer books must be handed to the supervisor-in-charge promptly. Failure to comply with this regulation will be cause for rejection of an answer paper.
(11) If during the course of an examination a student becomes ill or receives word of a domestic affliction, the student should report at once to the supervisor, hand in the unfinished paper and request that it be cancelled. If physical and/or emotional ill health is the cause, the student must report at once to a physican/counsellor so that subsequent application for a deferred examination is supported by a completed Physician/Counsellor Statement form. Students can consult professionals at University Health Services or Counselling and Student Development Centre during normal working hours or consult their physician/counsellor in the community. **Once an examination has been handed in for marking a student cannot request that the examination be cancelled for whatever reason. Such a request will be denied. Retroactive withdrawals will also not be considered.**

1. **[12 marks total.]** *Questions about number representations, arithmetic, and ROM arrays.*

   (a) **[2 marks.]** Convert $A0A_{16}$ to octal representation.

   $A0A_{16} = 1010\,0000\,1010_2 = 101\,000\,001\,010_2 = 5012_8$

   (b) **[2 marks.]** Convert $A0A_{16}$ to decimal representation.

   $A0A_{16} = 10 \times 16^2 + 0 \times 16^1 + 10 \times 16^0 = 2560 + 0 + 10 = 2570_{10}$

   (c) **[3 marks.]** In a 8-bit two's-complement system, what decimal number does the bit pattern 10000111 represent?

   The number is negative. Its magnitude can be found with two's-complement negation . . .

   invert bits of number: 0111 1000
   add 1: 0111 1001

   The magnitude is $2^6 + 2^5 + 2^4 + 2^3 + 2^0 = 64 + 32 + 16 + 8 + 1 = 121_{10}$.

   The bit pattern represents the number -121_{10}.

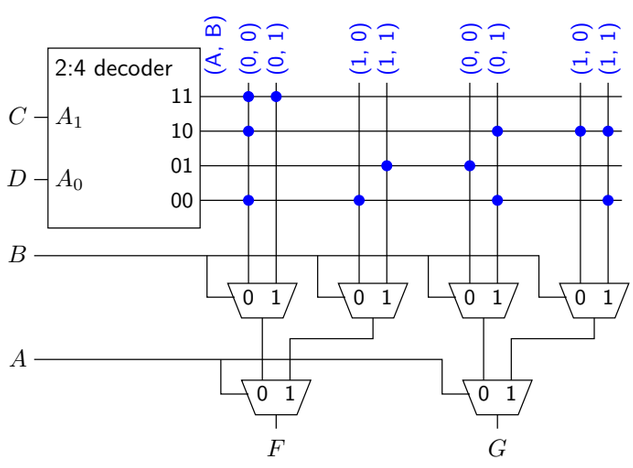
   (d) **[1 mark.]** Here is a 4-bit binary addition:

carries:	1	1000
a:		1101
b:		1100
sum:		1001

   Is there signed overflow in the addition? Give a clear reason for your answer.

   Answer: No. Reason: The signs of a, b and sum are all the same. Alternate reason: The carry out of the MSB column matches the carry in to the MSB column.

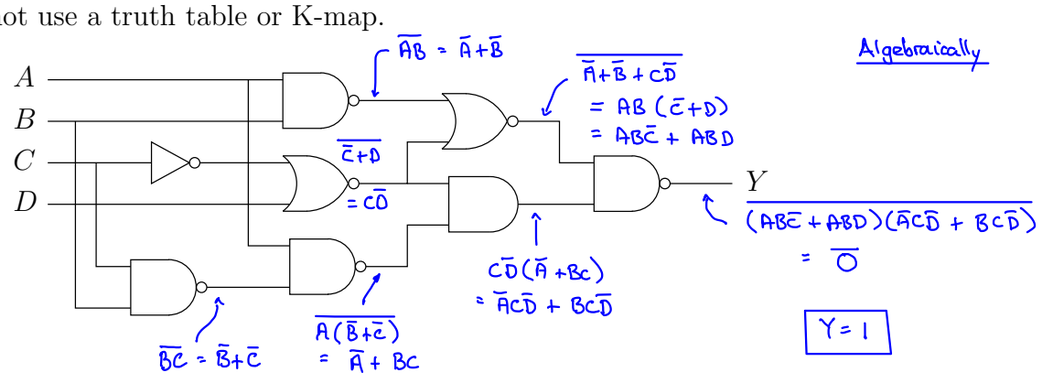
   (e) **[4 marks.]** The following circuit is made from a 4×8 ROM array and six 2:1 multiplexers. Place dots on the ROM array to implement the given truth table.



A	B	C	D	F	G	A	B	C	D	F	G
0	0	0	0	1	0	1	0	0	0	1	0
0	0	0	1	0	1	1	0	0	1	0	0
0	0	1	0	1	0	1	0	1	0	0	1
0	0	1	1	1	0	1	0	1	1	0	0
0	1	0	0	0	1	1	1	0	0	0	1
0	1	0	1	0	0	1	1	0	1	1	0
0	1	1	0	0	1	1	1	1	0	0	1
0	1	1	1	1	0	1	1	1	1	0	0

2. **[11 marks total.]** *Questions on Boolean algebra.*

(a) **[5 marks.]** Use algebra and/or bubble-pushing to determine Y. Express Y appropriately as either an SOP expression or as a constant (0 or 1). Do not use a truth table or K-map.



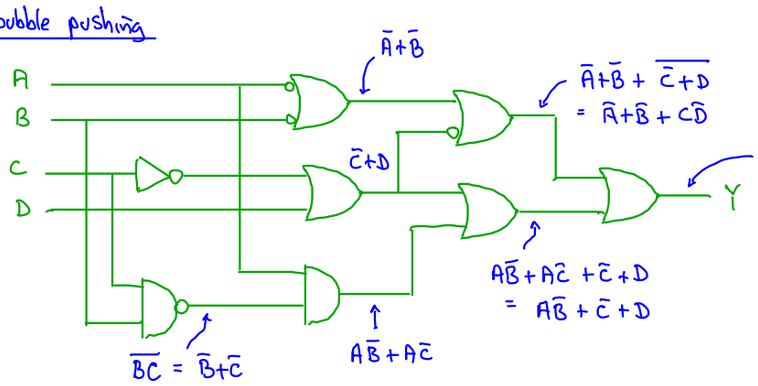
Algebraically

$\overline{\bar{A}+\bar{B}+C\bar{D}} = AB(\bar{C}+D) = AB\bar{C} + ABD$

$Y = \overline{(AB\bar{C}+ABD)(\bar{A}C\bar{D} + BC\bar{D})} = \overline{0}$

$Y = 1$

By bubble pushing



$A\bar{B} + \bar{C} + D + \bar{A} + \bar{B} + C\bar{D}$
$= \bar{A} + \bar{B} + \bar{C} + D + C\bar{D}$
$= \bar{A} + \bar{B} + \bar{C} + D + C$
$= 1$

$Y = 1$

(b) **[6 marks.]** Use algebraic manipulation and the definition of $A \oplus B$ as $\bar{A}B + A\bar{B}$ to answer the following questions. Do not use truth tables or K-maps.

i. Express $F = A \oplus B \oplus AB$ in minimal SOP form.

$F = A \oplus B \oplus AB = (A\bar{B} + \bar{A}B) \oplus AB$

$= (A\bar{B} + \bar{A}B)\overline{AB} + \overline{(A\bar{B} + \bar{A}B)}AB$

$= (A\bar{B} + \bar{A}B)(\bar{A}+\bar{B}) + (\bar{A}+B)(A+\bar{B})AB$

$= A\bar{B} + \bar{A}B + (\bar{A}\bar{B} + AB)AB$

$= A\bar{B} + \bar{A}B + AB$

$= A(\bar{B}+B) + \bar{A}B = A + \bar{A}B = (A+\bar{A})(A+B)$

so $F = A + B$

ii. Prove that the XOR operator is *distributive*; that is,

$$A(B \oplus C) = AB \oplus AC.$$

Left-hand side

$A(B \oplus C) = A(B\bar{C} + \bar{B}C)$

$= AB\bar{C} + A\bar{B}C$

Right-hand side

$AB \oplus AC = AB\overline{(AC)} + \overline{(AB)}AC$

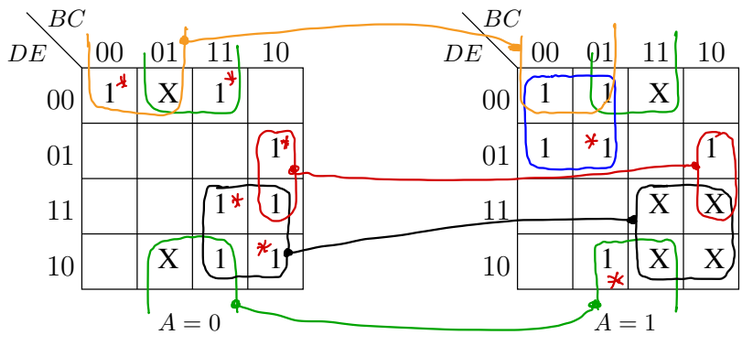
$= AB(\bar{A}+\bar{C}) + (\bar{A}+\bar{B})AC$

$= AB\bar{C} + A\bar{B}C$

$\therefore$ XOR operator is distributive

3. **[12 marks total.]** *K-map problems.*

(a) **[3 marks.]** Mark all the distinguished 1-cells with * on the 5-variable K-map below, and make a list of essential prime implicants.



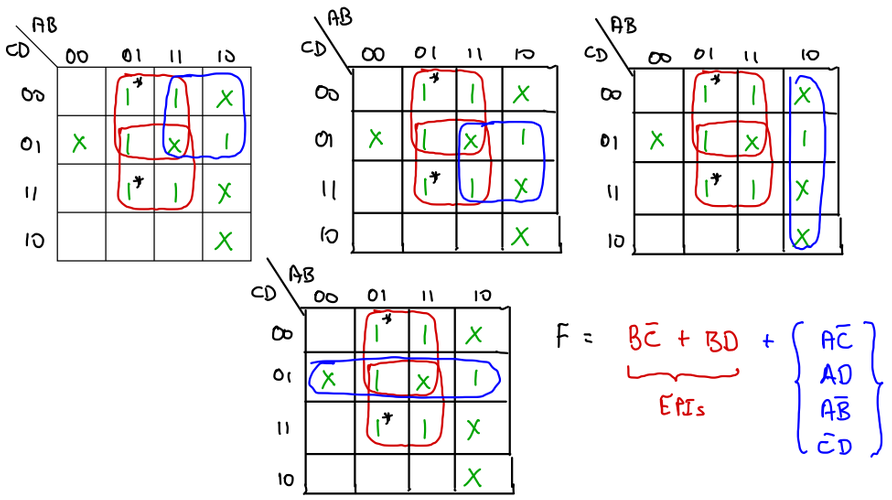
7 distinguished 1-cells. All prime implicants are essential.

$C\bar{E}$
$A\bar{B}\bar{D}$
BD
$B\bar{C}E$
$\bar{B}\bar{D}\bar{E}$

(b) **[4 marks.]** Consider the function F_1 given as a minterm list as follows:

$$F_1(A,B,C,D) = \sum(4,5,7,9,12,15) + X_1(A,B,C,D),$$

where $X_1(A,B,C,D) = \sum(1,8,10,11,13)$ are don't-cares. Use the blank K-map below to derive *all* possible minimal SOP expressions.

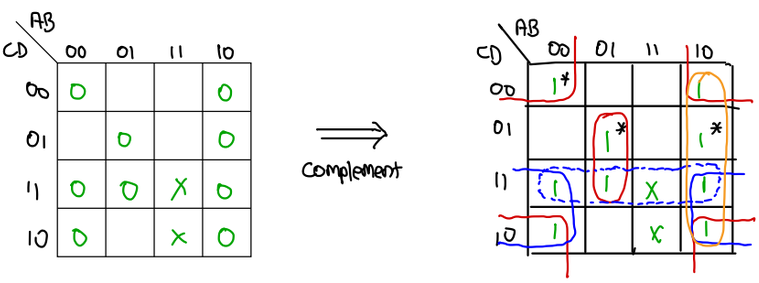


$F = \underbrace{B\bar{C} + BD}_{\text{EPIs}} + \left\{ \begin{matrix} A\bar{C} \\ AD \\ A\bar{B} \\ \bar{C}D \end{matrix} \right.$

(c) **[5 marks.]** Consider the function F_2 given as a maxterm list as follows:

$$F_2(A,B,C,D) = \left[\prod(0,2,3,5,7,8,9,10,11)\right] \cdot X_2(A,B,C,D),$$

where $X_2(A,B,C,D) = \prod(14,15)$ are don't-cares. Use the blank K-map below to derive *all* possible minimal POS expressions.

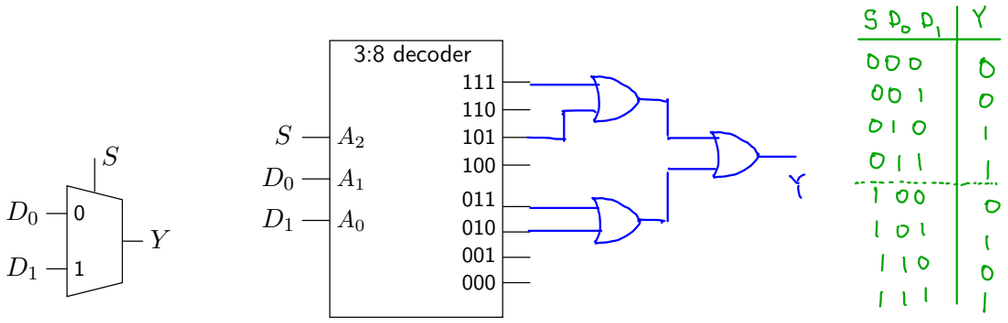


$\bar{F} = \underbrace{\bar{B}\bar{D} + A\bar{B} + \bar{A}BD}_{\text{EPIs}} + \left\{ \begin{matrix} CD \\ \bar{B}C \end{matrix} \right.$

giving $F = (B+D)(\bar{A}+B)(A+\bar{B}+\bar{D}) \left\{ \begin{matrix} (\bar{C}+\bar{D}) \\ (B+\bar{C}) \end{matrix} \right.$

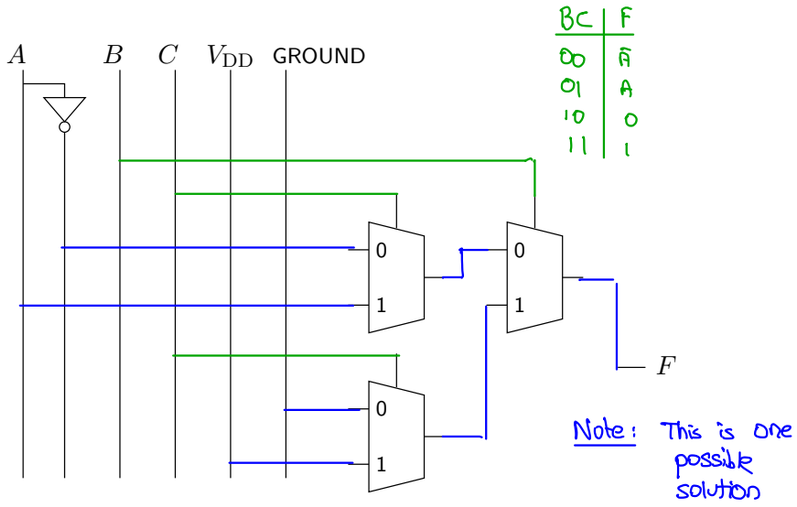
4. **[12 marks total.]** *Questions about multiplexers and decoders.*

(a) **[4 marks.]** Below on the left is the symbol for a 2:1 multiplexer, and a 3:8 decoder is shown on the right. Using this decoder, add wires and *only 2-input* OR *gates* to implement the 2:1 multiplexer.



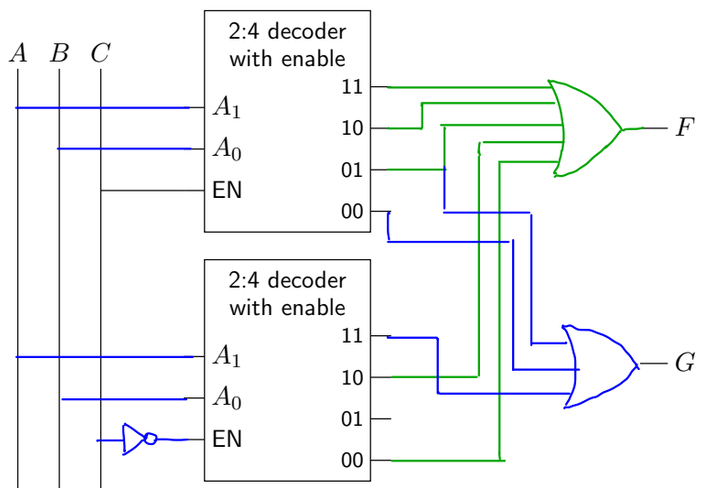
(b) **[4 marks.]** Shown below at right are three 2:1 multiplexers. Add wires—*but no additional logic elements*—to implement the function given in the truth table.

A	B	C	F
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1



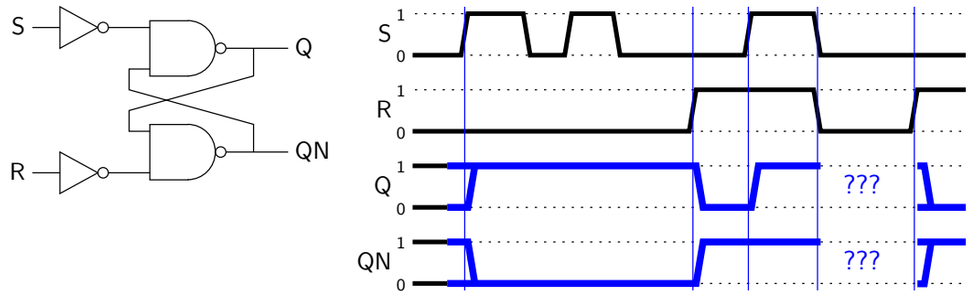
(c) **[4 marks.]** Shown below are two 2:4 decoders-with-enable. Add wires, one NOT gate, and two OR gates to implement the functions F and G given in the truth table.

A	B	C	F	G
0	0	0	1	0
0	0	1	0	1
0	1	0	0	0
0	1	1	1	1
1	0	0	1	0
1	0	1	1	0
1	1	0	0	1
1	1	1	1	0



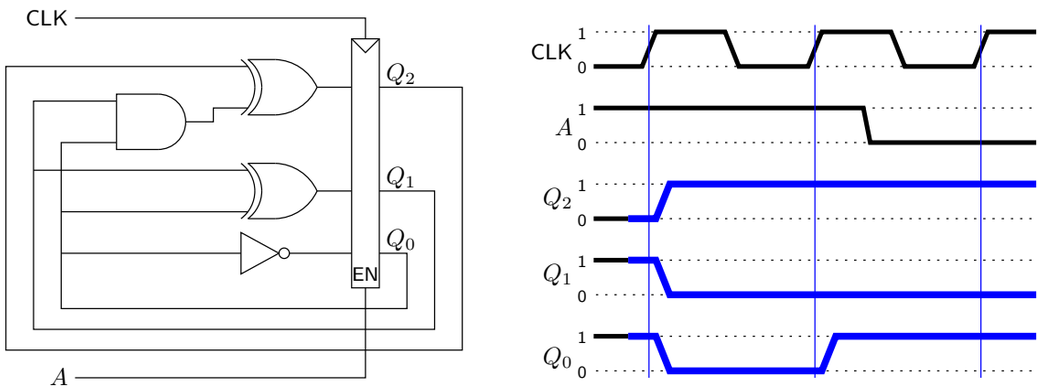
5. **[11 marks total.]** *Questions about sequential logic elements.*

(a) **[4 marks.]** The circuit below is a NAND-based SR latch. Complete the timing diagram, indicating clearly any intervals in time where it's not possible to know what the values of Q and QN are. Assume, as shown, that (Q, QN) could be either $(0, 1)$ or $(1, 0)$ at the start of the time interval being considered.



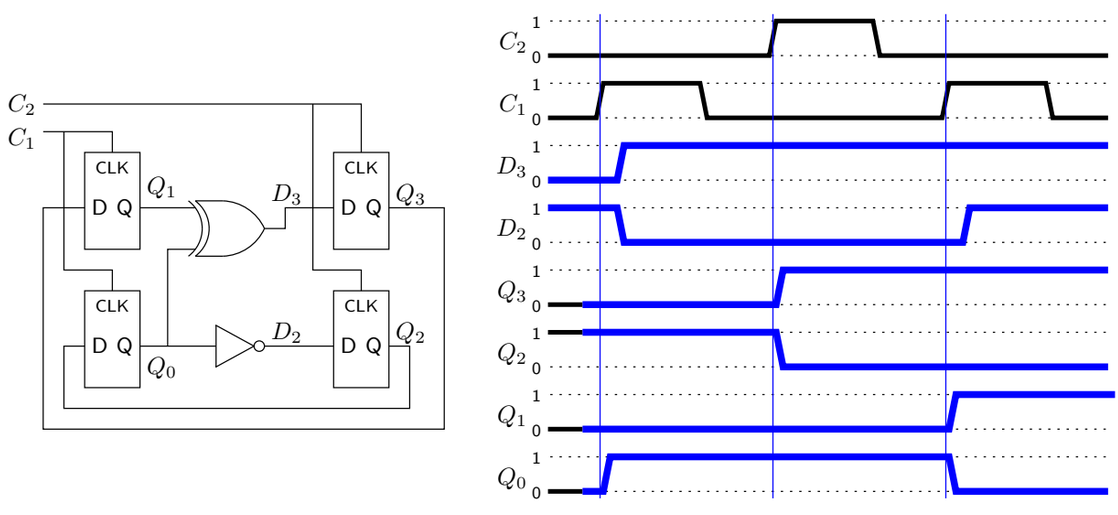
(Comment: It's *possible* that the circuit could go into a metastable state for some or all of the time interval marked with ???, but it's *not certain*.)

(b) **[4 marks.]** The EN (enable) input to the register in the circuit below affects all three flip-flops in the register the same way. Complete the timing diagram, assuming, as shown, that $(Q_2, Q_1, Q_0) = (0, 1, 1)$ at the start of the time interval being considered.



When EN = 1, $Q_2' = Q_2 \oplus (Q_1 Q_0)$, $Q_1' = Q_1 \oplus Q_0$, and $Q_0' = \overline{Q_0}$.
When EN = 0, $Q_2' = Q_2$, $Q_1' = Q_1$, and $Q_0' = Q_0$.

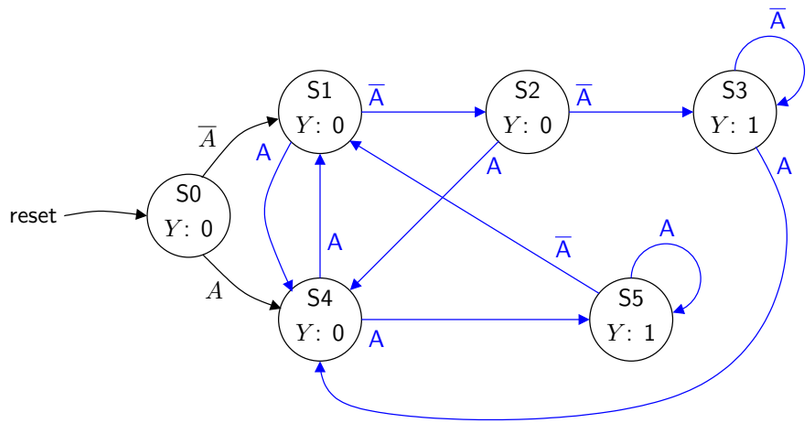
(c) **[3 marks.]** There are four D latches in the circuit shown below. Assume, as shown, that $(Q_3, Q_2, Q_1, Q_0) = (0, 1, 0, 0)$ at the start of the time interval being considered. Complete the timing diagram.



Values of D_3 and D_2 at the start of the time interval can be found using simple combinational expressions: $D_3 = Q_1 \oplus Q_0$ and $D_2 = \overline{Q_0}$.

6. **[13 marks total.]** *Design of a finite state machine (FSM).*

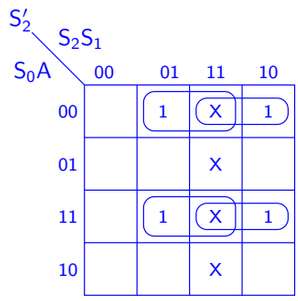
(a) **[5 marks.]** A Moore-type FSM is to have a 1-bit input A and a 1-bit output Y. Y should be 1 if and only if the values of A have been either 0-0-0 on the three most recent rising edges of CLK or 1-1 on the two most recent rising edges of CLK. Complete the following state transition diagram for the FSM.



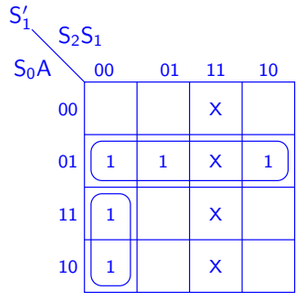
(b) **[8 marks.]** Using the given state encoding, find minimal SOP next-state and output equations for the FSM. Use don't-cares to help with minimization. In cases where there is more than one minimal SOP expression for a next state or an output, you only need to give one such expression.

state	S_2	S_1	S_0
S0	0	0	0
S1	0	0	1
S2	0	1	0
S3	1	0	0
S4	0	1	1
S5	1	0	1

current state and input	S_2	S_1	S_0	A	next state	S_2'	S_1'	S_0'
S0	0	0	0	0	S1	0	0	1
	0	0	0	1	S4	0	1	1
S1	0	0	1	0	S2	0	1	0
	0	0	1	1	S4	0	1	1
S2	0	1	0	0	S3	1	0	0
	0	1	0	1	S4	0	1	1
S4	0	1	1	0	S1	0	0	1
	0	1	1	1	S5	1	0	1
S3	1	0	0	0	S3	1	0	0
	1	0	0	1	S4	0	1	1
S5	1	0	1	0	S1	0	0	1
	1	0	1	1	S5	1	0	1
unused	1	1	0	0		X	X	X
states	1	1	0	1		X	X	X
	1	1	1	0		X	X	X
	1	1	1	1		X	X	X



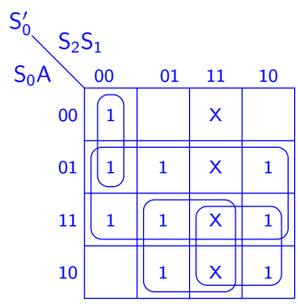
$S_2' = S_1\,\overline{S_0}\,\overline{A} + S_1\,S_0\,A + S_2\,\overline{S_0}\,\overline{A} + S_2\,S_0\,A$



$S_1' = \overline{S_0}\,A + \overline{S_2}\,\overline{S_1}\,S_0$

	S_2	S_1	S_0	Y
S0	0	0	0	0
S1	0	0	1	0
S2	0	1	0	0
S4	0	1	1	0
S3	1	0	0	1
S5	1	0	1	1
	1	1	0	X
	1	1	1	X

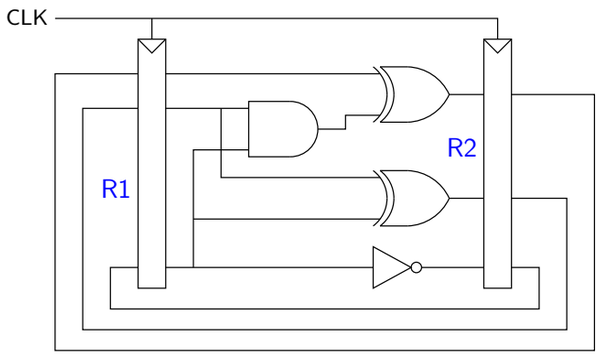
By inspection, $Y = S_2$



$S_0' = \overline{S_2}\,\overline{S_1}\,\overline{S_0} + A + S_1\,S_0 + S_2\,S_0$

7. **[10 marks total.]** *Questions about timing.*

Parts (a), (b) and (c) all concern the following synchronous circuit, which is supposed to run with a clock period of 300 ps. Timing parameters listed beside the schematic are in ps.



gate	t_{pd}	t_{cd}
NOT	21	14
AND2	63	42
XOR2	unknown	unknown

For both registers:

parameter	value
t_{setup}	57
t_{hold}	15
t_{pcq}	71
t_{ccq}	34

(a) **[3 marks.]** For reliable operation of the circuit, with zero clock skew, what is the maximum allowable t_{pd} for an XOR2 gate?

The critical path is from R1 to R2 through one AND2 and one XOR2.
$t_{pd\,AND2} + t_{pd\,XOR2} \leq T_C - t_{pcq} - t_{setup}$.
$t_{pd\,XOR2} \leq 300 - 71 - 57 - 63 = 109$ ps.

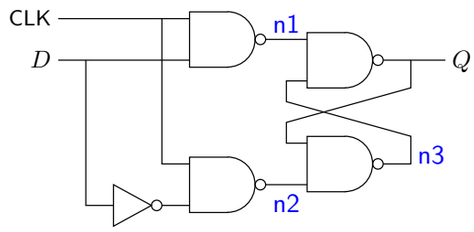
(b) **[2 marks.]** Repeat part (a), assuming now that t_{skew} is 20 ps.

The inequality for the critical path is now
$t_{pd\,AND2} + t_{pd\,XOR2} \leq T_C - t_{pcq} - t_{setup} - t_{skew}$.
Reusing the work in part (a), $t_{pd\,XOR2} \leq 109\,\text{ps} - 20\,\text{ps} = 89$ ps.

(c) **[2 marks.]** For avoidance of hold-time violations, what is the maximum allowable t_{skew}?

The short path is from R2 to R1 along a wire, for which t_{cd} is 0.
$t_{ccq} + t_{cd} \geq t_{hold} + t_{skew}$.
$t_{skew} \leq 34 + 0 - 15 = 19$ ps.

(d) **[3 marks.]** Consider the following design for a D latch and some related timing parameters.



gate	t_{pd}	t_{cd}
NOT	21 ps	14 ps
NAND2	37 ps	23 ps

Assume that Q and D have opposite values just before a rising edge of the clock, and D does not change in a way that causes a setup- or hold-time violation. Then t_{pcq} for the latch is defined to be the longest possible delay between the clock edge to a transition on Q, and t_{ccq} is defined to be the shortest possible such delay.

Find t_{pcq} and t_{ccq} for the latch. (Hint: Consider the case where $(D, Q) = (1, 0)$ before the clock edge separately from the case where $(D, Q) = (0, 1)$ before the clock edge.)

before CLK edge	transitions	delay
$(D, Q) = (1, 0)$	n1 $1 \to 0$, then Q $0 \to 1$	$2 \times$ NAND2
$(D, Q) = (0, 1)$	n2 $1 \to 0$, then n3 $0 \to 1$, then Q $1 \to 0$	$3 \times$ NAND2

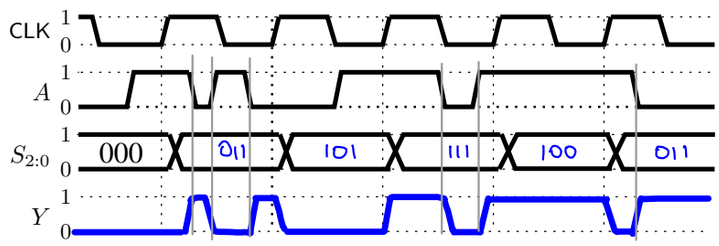
$t_{pcq} = 3 \times 37\,\text{ps} = 111$ ps and $t_{ccq} = 2 \times 23\,\text{ps} = 46$ ps.

(Comment: The NOT gate is not on *any* path from CLK to Q!)

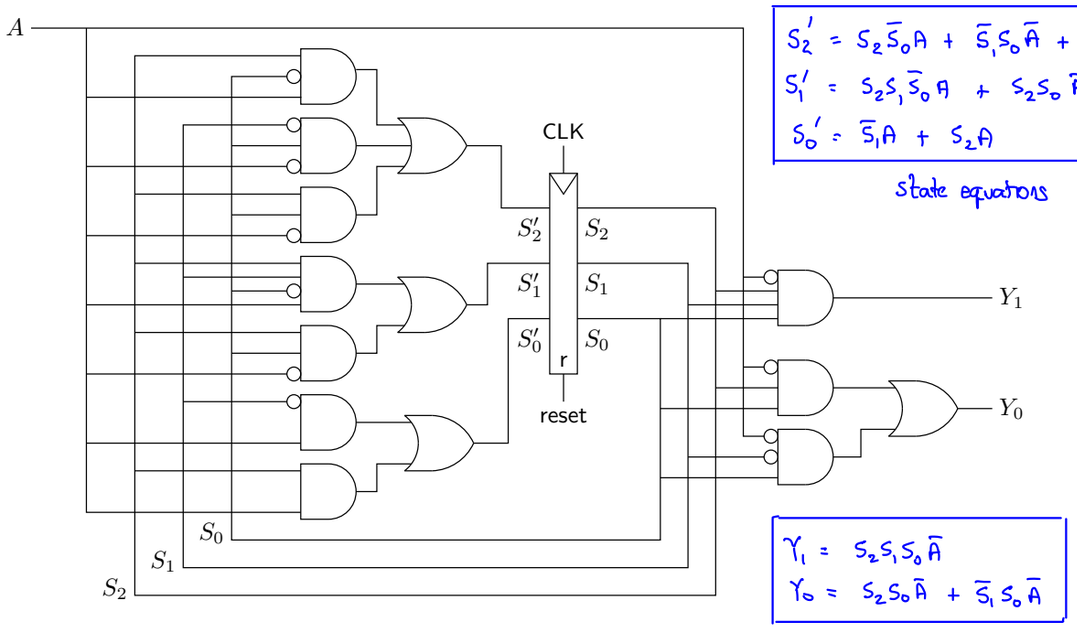
8. **[12 marks total.]** *Questions about FSM analysis.*

(a) **[4 marks.]** Below is the combined state and output table for a FSM that has a 1-bit input A, and a 1-bit output Y. The state variables are $S_{2:0}$. Complete the timing diagram at right using the information in this table.

$S_{2:0}$	A	$S'_{2:0}$	Y
000	0	000	0
000	1	011	0
011	0	101	1
011	1	011	0
100	0	101	0
100	1	011	1
101	0	011	0
101	1	111	0
111	0	101	0
111	1	100	1



(b) **[8 marks.]** Below is an FSM with a 1-bit input A, and a 2-bit output $Y_{1:0}$. Determine the combined state and output table, identify the unreachable states, and sketch the state-transition diagram. In your table, use 0's and 1's for the states and next states, not symbols like S0, S1, etc.



$S_2' = S_2\bar{S}_0A + \bar{S}_1S_0\bar{A} + S_2S_0\bar{A}$

$S_1' = S_2S_1\bar{S}_0A + S_2S_0\bar{A}$

$S_0' = \bar{S}_1A + S_2A$

state equations

$Y_1 = S_2S_1S_0\bar{A}$

$Y_0 = S_2S_0\bar{A} + \bar{S}_1S_0\bar{A}$

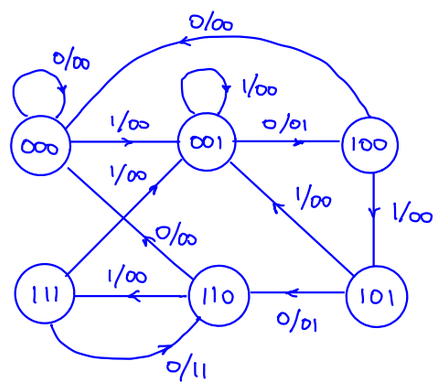
output equations

state transition table

$S_2S_1S_0$	A	$S_2'S_1'S_0'$	Y_1 Y_0
000	0	000	0 0
000	1	001	0 0
001	0	100	0 1
001	1	001	0 0
010	0	000	0 0
010	1	000	0 0
011	0	000	0 0
011	1	000	0 0
100	0	000	0 0
100	1	101	0 0
101	0	110	0 1
101	1	001	0 0
110	0	000	0 0
110	1	111	0 0
111	0	110	1 1
111	1	001	0 0

unreachable states

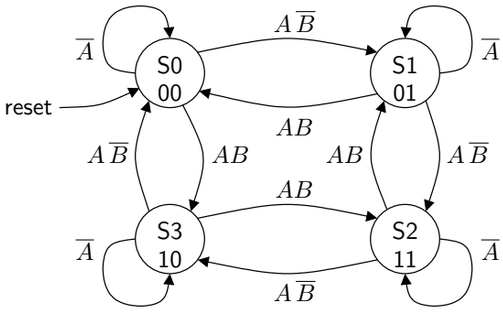
Mealy-style state transition diagram

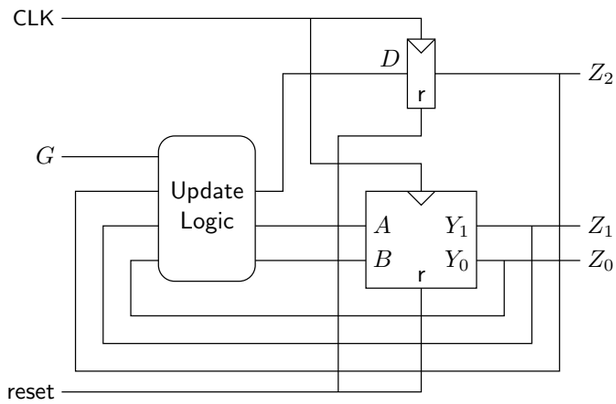


9. **[10 marks.]** *A problem about factored FSM design.*

This problem is about the design of a synchronous sequential circuit with a 1-bit input G (for "go") and a 3-bit output $Z_{2:0}$. When $G = 1$, $Z_{2:0}$ advances through the 3-bit Gray code cycle: 000, 001, 011, 010, 110, 111, 101, 100, 000, 001, ..., with updates on each rising edge of the clock. When $G = 0$, $Z_{2:0}$ is frozen—it does not change on a rising edge of the clock.

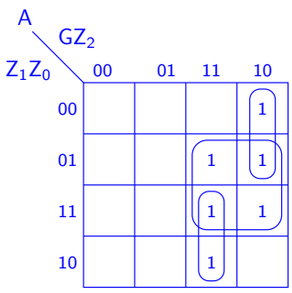
The circuit must be built using a resettable DFF, an FSM with a 2-bit state, and some combinational logic. Here are a state transition diagram for the 2-bit FSM and a schematic for the complete circuit:



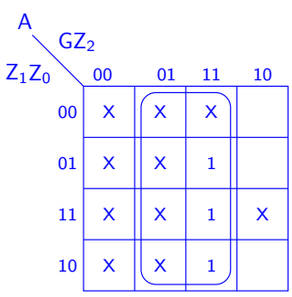


Fill in the truth table for the Update Logic and then find minimal SOP expressions for A, B and D. Note that don't-care output values may help in simplifying one or more of the SOP expressions.

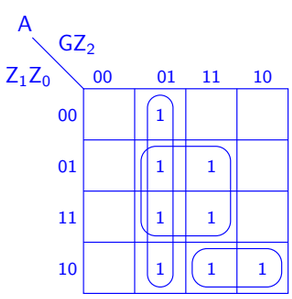
G	Z_2	Z_1	Z_0	A	B	D
0	0	0	0	0	X	0
0	0	0	1	0	X	0
0	0	1	0	0	X	0
0	0	1	1	0	X	0
0	1	0	0	0	X	1
0	1	0	1	0	X	1
0	1	1	0	0	X	1
0	1	1	1	0	X	1
1	0	0	0	1	0	0
1	0	0	1	1	0	0
1	0	1	0	0	X	1
1	0	1	1	1	0	0
1	1	0	0	0	X	0
1	1	0	1	1	1	1
1	1	1	0	1	1	1
1	1	1	1	1	1	1



$A = G\,\overline{Z_2}\,\overline{Z_1} + G\,Z_0 + G\,Z_1\,Z_2$



$B = Z_2$



$D = \overline{G}\,Z_2 + Z_2\,Z_0 + G\,Z_1\,\overline{Z_0}$

When G = 0, A = 0 to freeze the FSM state and D = Z_2 to freeze the DFF.
When G = 1, this table shows how to choose A, B and D:

$Z_{2:0}$	action
000, 001, or 011	go clockwise in FSM, freeze DFF
010	freeze FSM, change DFF state from 0 to 1
100	freeze FSM, change DFF state from 1 to 0
101, 110, or 111	go counterclockwise in FSM, freeze DFF