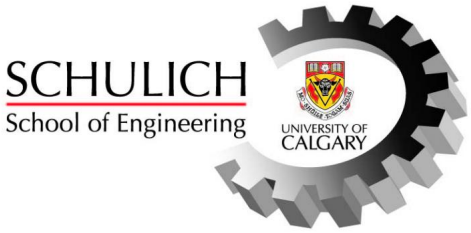
*Name:* _____

Lecture Section: _____
**L01** – N. Bartley 11:00-11:50
**L02** – S. Norman, 12:00-12:50




DEPARTMENT OF ELECTRICAL
AND COMPUTER ENGINEERING

# ENEL 353 - Digital Circuits

# Midterm Examination

Wednesday, October 30, 2013

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**Instructions:**

- Time allowed is 90 minutes.
- In order to minimize distraction to your fellow students, you may not leave during the last 10 minutes of the examination.
- The examination is closed-book.
- Non-programmable calculators are permitted.
- The maximum number of marks is 50, as indicated; the midterm examination counts 20% toward the final grade.
- Please use a pen or heavy pencil to ensure legibility.
- Please answer questions in the spaces provided; if space is insufficient, please use the back of the pages.
- Please show your work; where appropriate, marks will be awarded for proper and well-reasoned explanations.

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*UCID:* _____

1. **[12 marks total.]**

   (a) **[2 marks.]** Use repeated division to convert $329_{10}$ to hexadecimal representation.

   (b) **[2 marks.]** Convert $275_8$ to decimal representation. Show your work.

   (c) **[2 marks.]** Convert $A7B_{16}$ to octal representation. Show your work.

   (d) **[3 marks.]** The 5-bit unsigned binary representation of $25_{10}$ is $11001_2$. Use this information to determine the following two bit patterns.

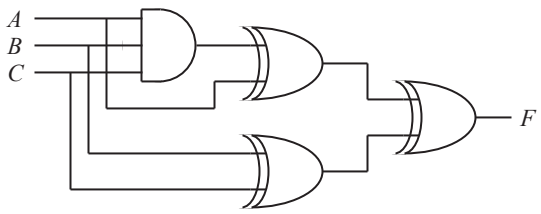
   6-bit two's complement representation of $-25_{10}$:

   8-bit sign/magnitude representation of $-25_{10}$:

   (e) **[3 marks.]** For each of the three additions below, answer YES or NO regarding unsigned and signed overflow, and briefly give a reason for each YES answer and for each NO answer. Marks will only be given if reasons are correct.

| | |
|---|---|
| *carries: 1 11110000*<br>a: 10011001<br>b: 01111000<br>*sum: 00010001* | *unsigned overflow?*<br><br>*signed overflow?* |
| *carries: 1 00000000*<br>a: 10100000<br>b: 11000000<br>*sum: 01100000* | *unsigned overflow?*<br><br>*signed overflow?* |
| *carries: 0 11110010*<br>a: 01101101<br>b: 01011001<br>*sum: 11000110* | *unsigned overflow?*<br><br>*signed overflow?* |

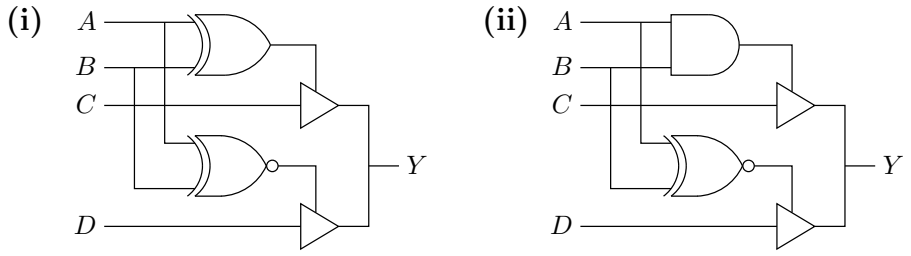
2. **[5 marks.]** Consider the circuit below.




Let $G = \bar{A}\bar{B}C + \bar{A}B\bar{C} + A\bar{B}\bar{C}$. By *algebraic manipulation*, prove or disprove that $F = G$. (Do not use a truth table or a K-map.)

3. **[8 marks total.]**

(a) **[3 marks.]**

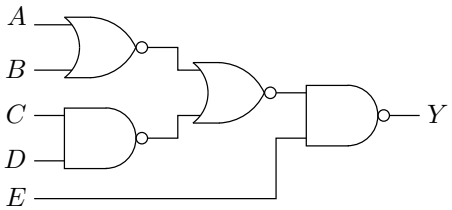



Check the box belonging to the correct statement:

- ☐ Contention is possible in circuit **(i)** but not in circuit **(ii)**.
- ☐ Contention is possible in circuit **(ii)** but not in circuit **(i)**.
- ☐ Contention is possible in both circuits.
- ☐ Contention is not possible in either circuit.

For full credit you must give a correct explanation for your answer in the space below.

(b) **[3 marks.]** Use bubble-pushing and/or algebra to find a sum-of-products expression for $Y$. If you use bubble-pushing, draw your equivalent circuit to the right of the given circuit.

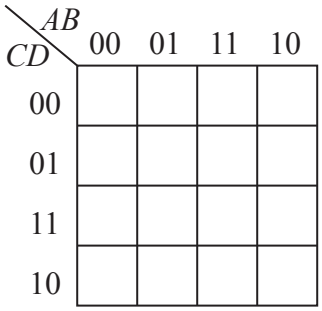


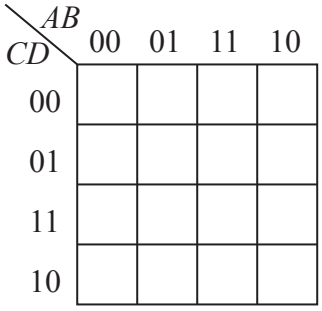

(c) **[2 marks.]** Suppose that $\bar{A}C + BD + A\bar{B}\bar{D}$ is a minimal sum-of-products expression for some logic function $F$. Use that information and some algebra to find a minimal product-of-sums expression for $\overline{F}$.

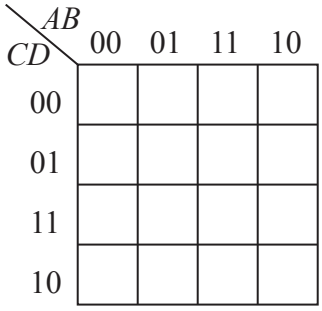
4. **[11 marks total.]**

(a) **[8 marks.]** Consider the function $F$ given in the truth table below. Use the blank K-maps to derive *all* minimum SOP and POS expressions for $F$. Indicate all essential prime implicants for $F$ or $\bar{F}$ in your maps. You may add more maps if you need them.

| $A$ | $B$ | $C$ | $D$ | $Y$ |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 1 |
| 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 1 | 0 | 0 |
| 0 | 0 | 1 | 1 | X |
| 0 | 1 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 | X |
| 0 | 1 | 1 | 0 | 1 |
| 0 | 1 | 1 | 1 | X |
| 1 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 0 |
| 1 | 0 | 1 | 1 | X |
| 1 | 1 | 0 | 0 | 0 |
| 1 | 1 | 0 | 1 | 0 |
| 1 | 1 | 1 | 0 | X |
| 1 | 1 | 1 | 1 | 1 |



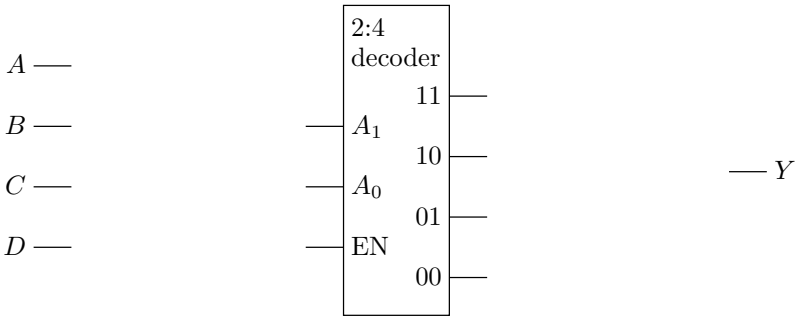

(b) **[3 marks.]** Sketch a two-level NOR-NOR circuit for a minimal POS expression from part (a). If you found more than one minimal POS expression in part (a), state which one you have chosen to implement. Assume that inputs $A$, $B$, $C$ and $D$ are available in true and complementary forms. There is no restriction on the number of inputs on each NOR gate.

5. **[9 marks total.]**

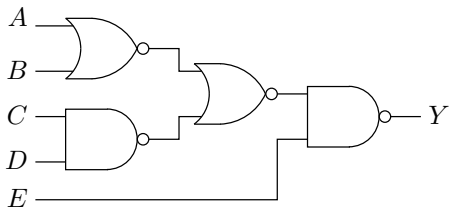
(a) **[3 marks.]** Draw a schematic to show how the function given in the truth table can be implemented with a 4:1 multiplexer, *one* inverter, and no other components. Show any intermediate work you had to do to design the circuit.

| $A$ | $B$ | $C$ | $Y$ |
|---|---|---|---|
| 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 0 |

(b) **[3 marks.]** Show how the function $Y = A(B \oplus C)D$ can be implemented using a 2:4 decoder with an enable input, *one* AND gate, *one* OR gate, and no other components. Express your answer by adding gates and wires to the schematic below.




(c) **[3 marks.]** Consider the following circuit and information about $t_{pd}$ (propagation delay) and $t_{cd}$ (contamination delay) for NAND and NOR gates.




| gate | $t_{pd}$ | $t_{cd}$ |
|---|---|---|
| NAND | 33 ps | 27 ps |
| NOR | 40 ps | 34 ps |

Determine the overall $t_{pd}$ and $t_{cd}$ for the circuit. Briefly explain how you got your answers.

6. **[5 marks.]** Consider the following 5-variable K-map for $F(A, B, C, D, E)$. Use the K-map to find a minimal SOP expression for $F$.

| $DE$ \ $BC$ | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 00 | | | | 1 |
| 01 | 1 | 1 | | 1 |
| 11 | 1 | 1 | 1 | 1 |
| 10 | | | | |

$A = 0$

| $DE$ \ $BC$ | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 00 | | | 1 | 1 |
| 01 | 1 | | | 1 |
| 11 | 1 | | 1 | 1 |
| 10 | | | 1 | |

$A = 1$

**Name (printed):**

**U of Calgary ID number:**

**Section (L01 is 11:00–11:50 with N. Bartley, L02 is 12:00–12:50 with S. Norman):**

| Problem | Mark |
|---|---|
| 1 | / 12 |
| 2 | / 5 |
| 3 | / 8 |
| 4 | / 11 |
| 5 | / 9 |
| 6 | / 5 |
| TOTAL | / 50 |