Name: Solutions

Lecture Section:
L01 – N. Bartley 11:00-11:50
L02 – S. Norman, 12:00-12:50

SCHULICH School of Engineering
UNIVERSITY OF CALGARY

DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING

ENEL 353 - Digital Circuits

Midterm Examination

Wednesday, October 30, 2013

Instructions:

- Time allowed is 90 minutes.
- In order to minimize distraction to your fellow students, you may not leave during the last 10 minutes of the examination.
- The examination is closed-book.
- Non-programmable calculators are permitted.
- The maximum number of marks is 50, as indicated; the midterm examination counts 20% toward the final grade.
- Please use a pen or heavy pencil to ensure legibility.
- Please answer questions in the spaces provided; if space is insufficient, please use the back of the pages.
- Please show your work; where appropriate, marks will be awarded for proper and well-reasoned explanations.

UCID: ____________

1. **[12 marks total.]**

   (a) **[2 marks.]** Use repeated division to convert 329_{10} to hexadecimal representation.

	quotient	remainder
329/16	20	9
20/16	1	4
1/16	0	1

answer: 149_{16}

   (b) **[2 marks.]** Convert 275_8 to decimal representation. Show your work.

$$275_8 = 2 \times 8^2 + 7 \times 8 + 5 = 128 + 56 + 5 = 189_{10}$$

   (c) **[2 marks.]** Convert A7B_{16} to octal representation. Show your work.

$$\overbrace{1010}^{A}\ \overbrace{0111}^{7}\ \overbrace{1011}^{B} = \underbrace{101}_{5}\ \underbrace{001}_{1}\ \underbrace{111}_{7}\ \underbrace{011}_{3}$$

answer: 5173_8

   (d) **[3 marks.]** The 5-bit unsigned binary representation of 25_{10} is 11001_2. Use this information to determine the following two bit patterns.

6-bit two's complement representation of -25_{10}:

6-bit $+25_{10}$: 011001
invert bits 100110
add 1 + 1
answer: 100111

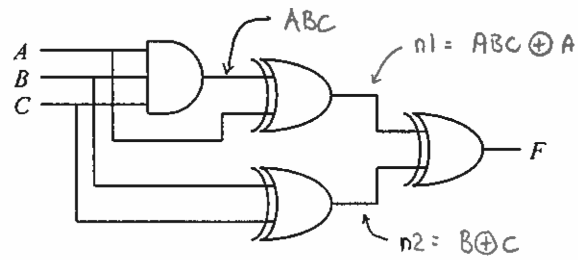
8-bit sign/magnitude representation of -25_{10}:

$\underbrace{1}_{\text{sign}}\ \underbrace{0011001}_{\text{7-bit magnitude}}$

   (e) **[3 marks.]** For each of the three additions below, answer YES or NO regarding unsigned and signed overflow, and briefly give a reason for each YES answer and for each NO answer. Marks will only be given if reasons are correct.

carries: 1 11110000 a: 10011001 b: 01111000 *sum:* 00010001	*unsigned overflow?* YES. C_{OUT} from MSB = 1. Another reason: sum < a. *signed overflow?* NO. Impossible when a, b have opposite signs Another reason: Circled carries are equal.
carries: 1 00000000 a: 10100000 b: 11000000 *sum:* 01100000	*unsigned overflow?* YES: C_{OUT} from MSB = 1. Another reason: sum < a. *signed overflow?* YES. a, b negative, sum positive. Another reason: Circled carries are not equal.
carries: 0 11110010 a: 01101101 b: 01011001 *sum:* 11000110	*unsigned overflow?* NO. C_{OUT} from MSB = 0. Another reason: sum ≥ a. *signed overflow?* YES. a, b positive, sum negative. Another reason: Circled carries are not equal.

2. **[5 marks.]** Consider the circuit below.



Let $G = \bar{A}\bar{B}C + \bar{A}B\bar{C} + A\bar{B}\bar{C}$. By *algebraic manipulation*, prove or disprove that $F = G$. (Do not use a truth table or a K-map.)

At n1: $n1 = ABC \oplus A = \overline{ABC} \cdot A + \cancelto{0}{ABC \cdot \bar{A}}$
$= (\bar{A} + \bar{B} + \bar{C})A = A\bar{B} + A\bar{C}$

At n2: $n2 = B \oplus C = B\bar{C} + \bar{B}C$

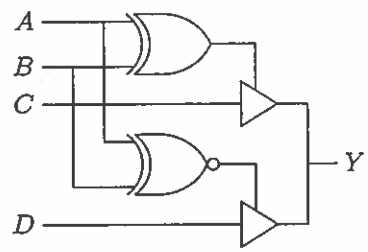
Then: $Y = n1 \oplus n2 = \overline{(A\bar{B} + A\bar{C})}(B\bar{C} + \bar{B}C) + (A\bar{B} + A\bar{C})\overline{(B\bar{C} + \bar{B}C)}$
$= (\overline{A\bar{B}})(\overline{A\bar{C}})(B\bar{C} + \bar{B}C) + (A\bar{B} + A\bar{C})(\overline{B\bar{C}})(\overline{\bar{B}C})$
$= (\bar{A} + B)(\bar{A} + C)(B\bar{C} + \bar{B}C) + (A\bar{B} + A\bar{C})(\bar{B} + C)(B + \bar{C})$
$= (\bar{A} + \bar{A}C + \bar{A}B + BC)(B\bar{C} + \bar{B}C) + (A\bar{B} + A\bar{C})(\bar{B}\bar{C} + BC)$
$= [\bar{A}(1 + C + B) + BC](B\bar{C} + \bar{B}C) + (A\bar{B} + A\bar{C})(\bar{B}\bar{C} + BC)$

$= (\bar{A} + BC)(B\bar{C} + \bar{B}C) + A\bar{B}\bar{C} + A\bar{B}\bar{C}$
$= \bar{A}B\bar{C} + \bar{A}\bar{B}C + A\bar{B}\bar{C}$

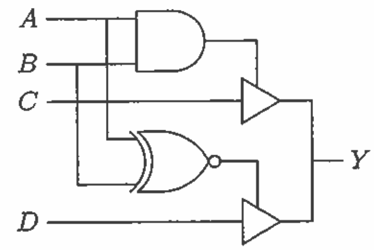
3. **[8 marks total.]**

(a) **[3 marks.]**

(i)



(ii)



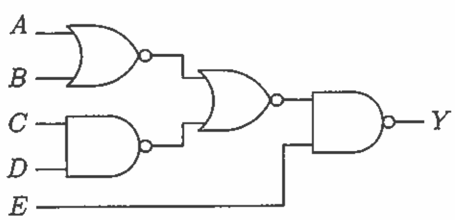
Check the box belonging to the correct statement:

- ☐ Contention is possible in circuit (i) but not in circuit (ii).
- ☑ Contention is possible in circuit (ii) but not in circuit (i).
- ☐ Contention is possible in both circuits.
- ☐ Contention is not possible in either circuit.

For full credit you must give a correct explanation for your answer in the space below.

In (i) $\text{XNOR}(A,B) = \overline{\text{XOR}(A,B)}$, so only one tristate is enabled at any given time. In (ii) both tristates are enabled when $A=B=1$, so there is contention when $A=B=1$, $C \neq D$.

(b) **[3 marks.]** Use bubble-pushing and/or algebra to find a sum-of-products expression for Y. If you use bubble-pushing, draw your equivalent circuit to the right of the given circuit.

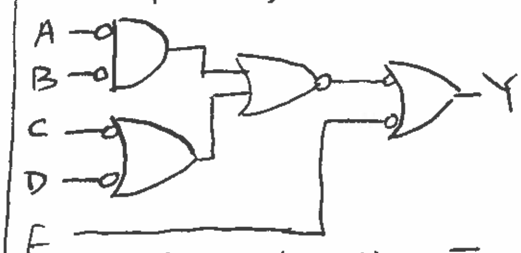


Algebra

$$Y = \overline{\left(\overline{\overline{(A+B)} + \overline{(CD)}}\right) E} = \left(\overline{(A+B)} + \overline{CD}\right) + \overline{E}$$

$$= \overline{A}\,\overline{B} + \overline{C} + \overline{D} + \overline{E}$$

Bubble-pushing



$$Y = (\overline{A}\overline{B} + (\overline{C}+\overline{D})) + \overline{E}$$

$$= \overline{A}\overline{B} + \overline{C} + \overline{D} + \overline{E}$$

(c) **[2 marks.]** Suppose that $\bar{A}C + BD + A\bar{B}\bar{D}$ is a minimal sum-of-products expression for some logic function F. Use that information and some algebra to find a minimal product-of-sums expression for $\overline{F}$.

$$\overline{F} = \overline{(\overline{A}C + BD + A\overline{B}\,\overline{D})}$$

$$= \overline{(\overline{A}C)}\;\overline{(BD)}\;\overline{(A\overline{B}\,\overline{D})}$$

$$= (A+\overline{C})(\overline{B}+\overline{D})(\overline{A}+B+D)$$

(Remark, not required as part of answer: The above POS for $\overline{F}$ must be minimal, because if it were not, the given SOP for F could not be minimal.)

4. **[11 marks total.]**

(a) **[8 marks.]** Consider the function F given in the truth table below. Use the blank K-maps to derive *all* minimum SOP and POS expressions for F. Indicate all essential prime implicants for F or $\bar{F}$ in your maps. You may add more maps if you need them.

A	B	C	D	Y
0	0	0	0	1
0	0	0	1	1
0	0	1	0	0
0	0	1	1	X
0	1	0	0	0
0	1	0	1	X
0	1	1	0	1
0	1	1	1	X
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	X
1	1	0	0	0
1	1	0	1	0
1	1	1	0	X
1	1	1	1	1

CD \ AB	00	01	11	10
00	1*			
01	1	X		
11	X	X	1	X
10		1*	X	

$\bar{A}\bar{B}\bar{C}$

BC

$F = \bar{A}\bar{B}\bar{C} + BC$

(both are EPIs)

CD \ AB	00	01	11	10
00		1*	1	1
01		X	1	1
11	X	X		X
10	1*		X	1

$A\bar{C}$

$B\bar{C}$

$\bar{B}C$

$\bar{F} = A\bar{C} + \underbrace{B\bar{C} + \bar{B}C}_{\text{EPIs}}$

$F = (\overline{A\bar{C}})(\overline{B\bar{C}})(\overline{\bar{B}C})$
$= (\bar{A}+C)(\bar{B}+C)(B+\bar{C})$

CD \ AB	00	01	11	10
00		1*	1	1
01		X	1	1
11	X	X		X
10	1*		X	1

$B\bar{C}$

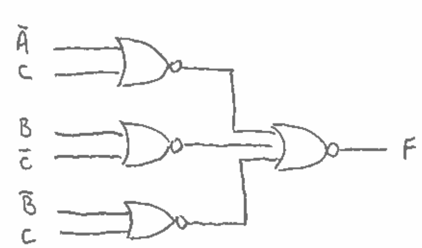
$A\bar{B}$

$\bar{B}C$

$\bar{F} = A\bar{B} + \underbrace{B\bar{C} + \bar{B}C}_{\text{EPIs}}$

$F = (\overline{A\bar{B}}) \cdot (\overline{B\bar{C}}) \cdot (\overline{\bar{B}C})$
$= (\bar{A}+B)(\bar{B}+C)(B+\bar{C})$

(b) **[3 marks.]** Sketch a two-level NOR-NOR circuit for a minimal POS expression from part (a). If you found more than one minimal POS expression in part (a), state which one you have chosen to implement. Assume that inputs A, B, C and D are available in true and complementary forms. There is no restriction on the number of inputs on each NOR gate.



First POS expression:

$F = (\bar{A}+C)(\bar{B}+C)(B+\bar{C})$

$= \overline{\overline{(\bar{A}+C)} + \overline{(\bar{B}+C)} + \overline{(B+\bar{C})}}$ (all NORs)

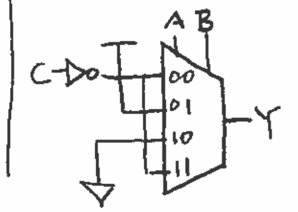
5. **[9 marks total.]**

(a) **[3 marks.]** Draw a schematic to show how the function given in the truth table can be implemented with a 4:1 multiplexer, *one* inverter, and no other components. Show any intermediate work you had to do to design the circuit.

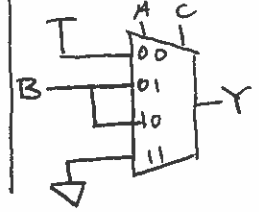
Any 1 of the 3 solutions is acceptable. As well, there are a few other unusual but correct solutions.

A	B	C	Y
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	0

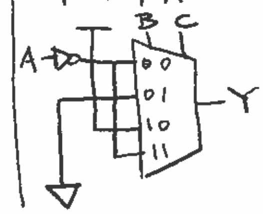
A	B	Y
0	0	$\overline{C}$
0	1	1
1	0	0
1	1	$\overline{C}$



A	C	Y
0	0	1
0	1	B
1	0	B
1	1	0



B	C	Y
0	0	$\overline{A}$
0	1	0
1	0	1
1	1	$\overline{A}$

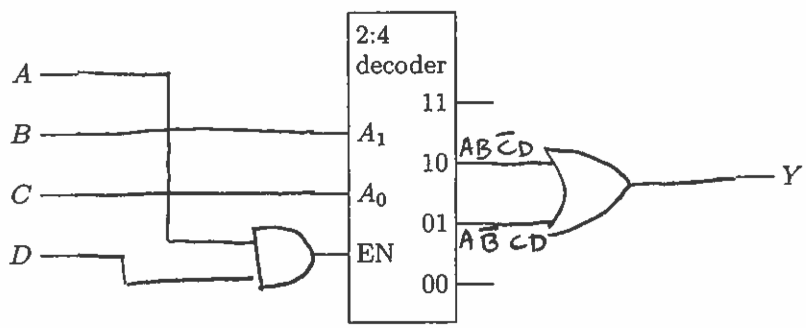


(b) **[3 marks.]** Show how the function $Y = A(B \oplus C)D$ can be implemented using a 2:4 decoder with an enable input, *one* AND gate, *one* OR gate, and no other components. Express your answer by adding gates and wires to the schematic below.

$A(B \oplus C)D$

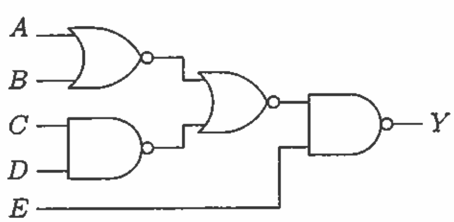
$= AD(B\overline{C} + \overline{B}C)$

$= A\overline{B}CD + AB\overline{C}D$



There are a few other correct solutions.

(c) **[3 marks.]** Consider the following circuit and information about t_{pd} (propagation delay) and t_{cd} (contamination delay) for NAND and NOR gates.



gate	t_{pd}	t_{cd}
NAND	33 ps	27 ps
NOR	40 ps	34 ps

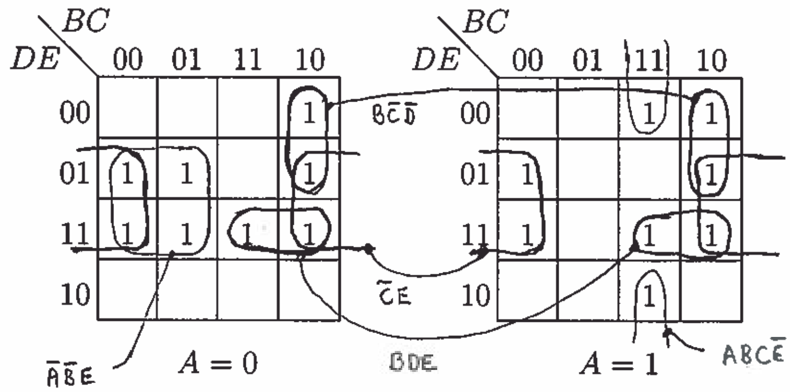
Determine the overall t_{pd} and t_{cd} for the circuit. Briefly explain how you got your answers.

t_{pd} Critical path is from A or B to Y, because the NORs in this circuit are slower than the NANDs.

Answer: $\underbrace{40\text{ps}}_{\text{NOR}} + \underbrace{40\text{ps}}_{\text{NOR}} + \underbrace{33\text{ps}}_{\text{NAND}} = \underline{113\text{ps}}$.

t_{cd} The short path is obviously E to Y. $t_{cd} = \underbrace{27\text{ps}}_{\text{one NAND}}$

6. **[5 marks.]** Consider the following 5-variable K-map for $F(A, B, C, D, E)$. Use the K-map to find a minimal SOP expression for F.



$$F = \bar{A}\bar{B}E + BDE + \bar{C}E + B\bar{C}\bar{D} + ABC\bar{E}$$

Name (printed):

U of Calgary ID number:

Section (L01 is 11:00–11:50 with N. Bartley, L02 is 12:00–12:50 with S. Norman):

Problem	Mark
1	/ 12
2	/ 5
3	/ 8
4	/ 11
5	/ 9
6	/ 5
TOTAL	/ 50