

NAME: Solutions

When you start the test, please repeat your name and add your U of C ID number at the bottom of the last page.



DEPARTMENT OF ELECTRICAL
AND COMPUTER ENGINEERING

ENEL 353: Digital Circuits
Midterm Examination
Wednesday, October 28, 2015

Instructions:

- Time allowed is 90 minutes.
 - In order to minimize distraction to your fellow students, you may not leave during the last 10 minutes of the examination.
 - The examination is closed-book.
 - Non-programmable calculators are permitted.
 - The maximum number of marks is 50, as indicated; the midterm examination counts 20% toward the final grade.
 - Please use a pen or heavy pencil to ensure legibility.
 - Please answer questions in the spaces provided; if space is insufficient, please use the back of the pages.
 - Please show your work; where appropriate, marks will be awarded for proper and well-reasoned explanations.
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1. [11 marks total.]

(a) [2 marks.] Use repeated division to convert 230_{10} to octal representation.

division	quotient	remainder
$230 \div 8$	28	6
$28 \div 8$	3	4
$3 \div 8$	0	3

Answer: 346_8

(b) [1 mark.] What is the value of $19D_{16}$ in base ten?

$$1 \times 16^2 + 9 \times 16^1 + 13 \times 16^0 = 413_{10}$$

(c) [3 marks.] Consider the bit pattern 100011.

(1 mark)

In a 6-bit sign/magnitude system, what number does the bit pattern represent?

Sign: negative
 magnitude: 3_{10}
 answer: -3_{10}

(2 marks)
 In a 6-bit two's complement system, what number does the bit pattern represent? Let x be the number

flip bits: 011100
 add 1: 011101

$-x$ is $2^4 + 2^3 + 2^2 + 2^0 = 29$, so $x = -29_{10}$

(d) [2 marks.] What is the six-bit sum generated by a six-bit adder when the inputs are 110100 and 100111, and what is the carry out of the most significant bit?

	1	001	000	← carries
		110	100	← a
		100	111	← b
		<hr/>		
		011	011	← sum

carry out of MSB.

(e) [1 mark.] If all the six-bit numbers in part (d) are interpreted as two's complement, was there overflow in the addition? Give a reason for your answer. Yes. a and b are negative, but sum is positive.

(Alternate reason: Carry in to MSB \neq Carry out of MSB.)

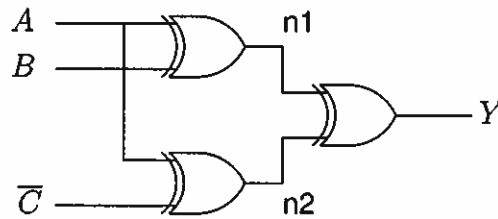
(f) [2 marks.] Half of the conversions from 3-bit unsigned binary to 3-bit Gray code are given below. Fill in the the table to the right with other half of the conversions.

unsigned binary	Gray code
000	000
001	001
010	011
011	010

unsigned binary	Gray code
100	110
101	111
110	101
111	100

2-bit Gray code, reverse order.

2. [6 marks.] Consider the circuit below.



Let $G = \overline{B}C + BC$. By algebraic manipulation, prove or disprove that $Y = G$. (Do not use a truth table or a K-map.)

$$\begin{aligned} n1 &= A \oplus B = \overline{A}B + A\overline{B} \\ n2 &= A \oplus \overline{C} = AC + \overline{A}\overline{C} \end{aligned}$$

$$\begin{aligned} \text{Then } Y &= n1 \oplus n2 = n1 \cdot \overline{n2} + \overline{n1} \cdot n2 \\ &= (\overline{A}B + A\overline{B})(\overline{AC + \overline{A}\overline{C}}) + (\overline{\overline{A}B + A\overline{B}})(AC + \overline{A}\overline{C}) \end{aligned}$$

Property of XOR:
 $\overline{A \oplus B} = A \oplus \overline{B}$
 $= \overline{A} \oplus B$



$$\begin{aligned} \overline{AC + \overline{A}\overline{C}} &= \overline{AC} \cdot \overline{\overline{A}\overline{C}} \\ &= (\overline{A} + \overline{C})(A + C) \\ &= \overline{A}A + \overline{A}C + A\overline{C} + \overline{C}C \\ &= \overline{A}C + A\overline{C} \end{aligned}$$

$$\begin{aligned} \overline{\overline{A}B + A\overline{B}} &= \overline{\overline{A}B} \cdot \overline{A\overline{B}} \\ &= (\overline{\overline{A}} + \overline{B})(\overline{A} + \overline{\overline{B}}) \\ &= \overline{\overline{A}} + \overline{B} + \overline{A} + \overline{\overline{B}} \\ &= \overline{\overline{A}} + \overline{B} + A + B \\ &= \overline{A} + \overline{B} + A + B \end{aligned}$$

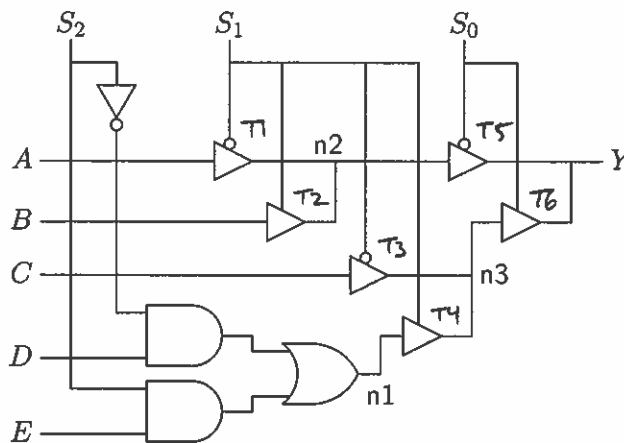
$$\begin{aligned} Y &= (\overline{A}B + A\overline{B})(\overline{A}C + A\overline{C}) + (\overline{\overline{A}B + A\overline{B}})(AC + \overline{A}\overline{C}) \\ &= \overline{A}B\overline{A}C + \overline{A}B A\overline{C} + \overline{A}B\overline{C} + \overline{A}B AC \\ &\quad + \overline{A}B\overline{A}C + \overline{A}B A\overline{C} + A\overline{B}\overline{C} + A\overline{B} AC \\ &= \overline{A}B\overline{C} + \overline{A}B C + \overline{A}B\overline{C} + A\overline{B} C \\ &= \overline{B}C(A + \overline{A}) + BC(\overline{A} + A) \end{aligned}$$

$$Y = \overline{B}C + BC$$

Therefore $Y = G$

3. [8 marks total.]

- (a) [2 marks.] Contention (or “fighting”) is sometimes possible when two gate outputs are wired together. In the circuit below, nodes n2, n3, and Y are each wired to the outputs of two different gates. Explain why contention is impossible in this particular circuit.



There is no contention at n₂ because S₁ can enable only one of T₁ or T₂. The same applies for n₃, S₁, T₃, T₄, and for Y, S₀, T₅, T₆.

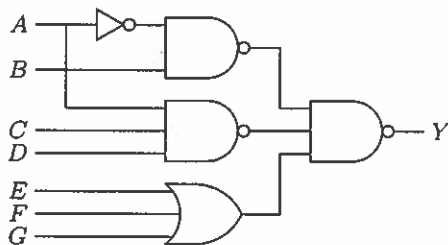
- (b) [3 marks.] Find an SOP expression for Y in the circuit of part (a), in terms of inputs A, B, C, D, E, S₂, S₁, and S₀.

The part of the circuit involving the tristate buffers is a 4:1 mux.

$$Y = \bar{S}_1 \bar{S}_0 A + S_1 \bar{S}_0 B + \bar{S}_1 S_0 C + S_1 S_0 (\bar{S}_2 D + S_2 E)$$

$$= \bar{S}_1 \bar{S}_0 A + S_1 \bar{S}_0 B + \bar{S}_1 S_0 C + \bar{S}_2 S_1 S_0 D + S_2 S_1 S_0 E$$

- (c) [3 marks.] Use bubble-pushing and/or algebra to find an SOP expression for Y in the circuit below. If you use bubble-pushing, draw an equivalent circuit beside the given circuit.



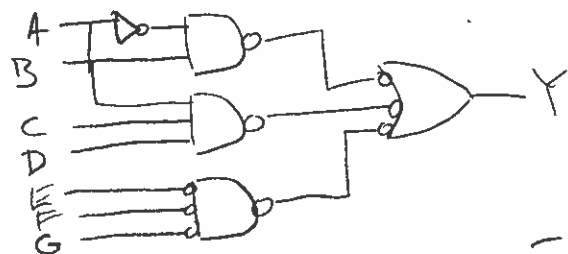
Algebra

$$Y = (\bar{A}B)(ACD)(E+F+G)$$

$$= \bar{A}B + ACD + \overline{(E+F+G)}$$

$$= \bar{A}B + ACD + \bar{E}\bar{F}\bar{G}$$

Bubble-pushing



$$Y = \bar{A}B + ACD + \bar{E}\bar{F}\bar{G}$$

4. [11 marks total.]

- (a) [8 marks.] Consider the function Y given in the truth table below. Use the blank K-maps to derive *all* minimum SOP and POS expressions for Y . Indicate all essential prime implicants for Y or \bar{Y} in your maps. You may add more maps if you need them.

A	B	C	D	Y
0	0	0	0	1
0	0	0	1	0
0	0	1	0	X
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	0
0	1	1	1	1
1	0	0	0	1
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0
1	1	0	0	X
1	1	0	1	0
1	1	1	0	1
1	1	1	1	X

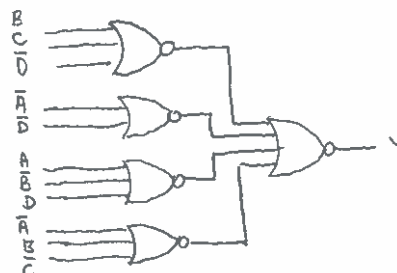
Four minimal SOP solutions
 $Y = \bar{A}BD + \bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}C + A\bar{B}\bar{D}$
 $Y = \bar{A}BD + \bar{B}\bar{C}\bar{D} + \bar{A}CD + A\bar{B}\bar{D}$
 $Y = \bar{A}BD + \bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}C + ABC$
 $Y = \bar{A}BD + \bar{B}\bar{C}\bar{D} + \bar{A}CD + ABC$

4 choices

Two minimal POS solutions
 $\bar{Y} = \bar{B}\bar{C}\bar{D} + AD + \bar{A}\bar{B}\bar{D} + \bar{A}\bar{B}C$
 $\rightarrow Y = (B+C+\bar{D})(\bar{A}+\bar{D})(A+\bar{B}+\bar{D})(\bar{A}+B+\bar{C})$
 $\bar{Y} = \bar{B}\bar{C}\bar{D} + AD + \bar{A}\bar{B}\bar{D} + \bar{B}\bar{C}\bar{D}$
 $\rightarrow Y = (B+C+\bar{D})(\bar{A}+\bar{D})(A+\bar{B}+\bar{D})(\bar{B}+\bar{C}+\bar{D})$

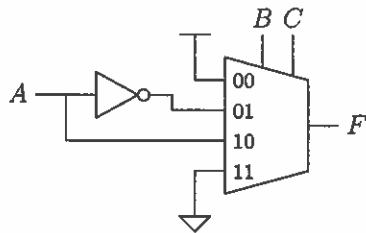
- (b) [3 marks.] Sketch a two-level NOR-NOR circuit for a minimal POS expression from part (a). Assume that A, B, C and D are available in true and complementary forms. There is no restriction on the number of inputs on each NOR gate.

First solution:
 $Y = (B+C+\bar{D})(\bar{A}+\bar{D})(A+\bar{B}+\bar{D})(\bar{A}+B+\bar{C})$



5. [9 marks total.]

(a) [3 marks.] Find a canonical SOP expression for $F(A, B, C)$. Show carefully how you obtained your expression.



B	C	F
00	01	1
10	11	0

A	B	C	F
0	0	0	1
0	0	1	$\bar{A} = 1$
0	1	0	$A = 0$
0	1	1	0
1	0	0	1
1	0	1	$\bar{A} = 0$
1	1	0	$A = 1$
1	1	1	0

Answer:

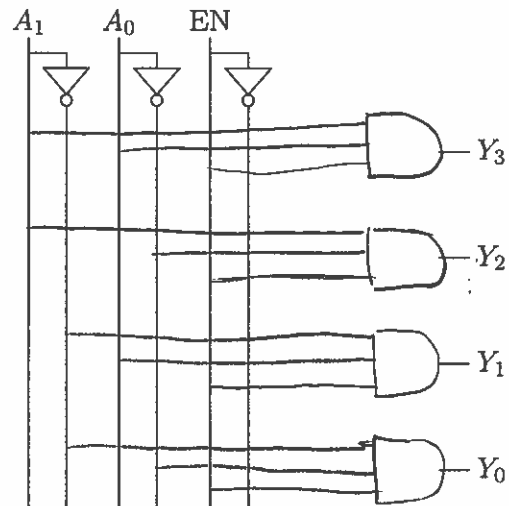
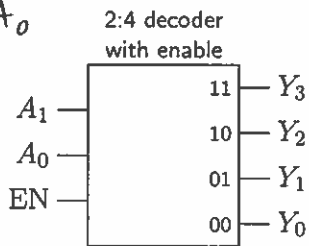
$$F = m_0 + m_1 + m_4 + m_6$$

$$= \bar{A}\bar{B}\bar{C} + \bar{A}\bar{B}C + A\bar{B}\bar{C} + A\bar{B}C$$

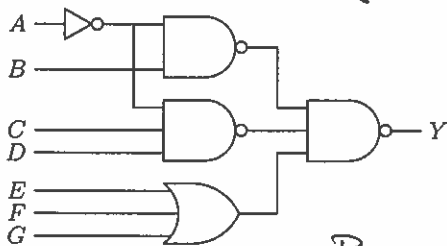
(b) [3 marks.] Below on the left is a symbol for a 2:4 decoder with an enable input. Show how such a circuit could be implemented by adding only wires and AND gates to the schematic below on the right.

Notes, not needed for marks...

- feed EN to AND gates to make all outputs 0 if EN = 0
- if EN = 1, outputs are minterms of A_1 and A_0



(c) [3 marks.] Use the data in the table to find the overall t_{pd} and overall t_{cd} for the given circuit. (2 marks for t_{pd} , 1 mark for t_{cd} .)



gate	t_{pd}	t_{cd}
NOT	18 ps	13 ps
OR	76 ps	51 ps
NAND2	39 ps	28 ps
NAND3	55 ps	37 ps

Short path

NAND2 + NAND3

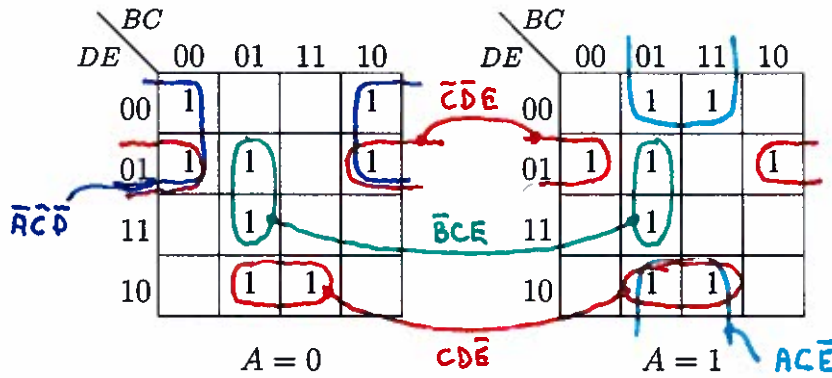
$$t_{cd} = 28 + 37 = \boxed{65 \text{ ps}}$$

Possible critical paths

NOT + NAND3 + NAND3: $18 + 55 + 55 = 128 \text{ ps}$
 OR + NAND3: $76 + 55 = 131 \text{ ps}$

Overall t_{pd} is $\boxed{131 \text{ ps}}$

6. [5 marks.] Use the following 5-variable K-map for $F(A, B, C, D, E)$, and find a minimal SOP expression for F .



One solution: $F = \bar{A}\bar{C}\bar{D} + \bar{B}CE + AC\bar{E} + \bar{C}\bar{D}E + C\bar{D}\bar{E}$

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question 1	question 2	question 3	question 4	question 5	question 6	TOTAL
/ 11	/ 6	/ 8	/ 11	/ 9	/ 5	/ 50