NAME: _____ **SECTION:** _____

L01: Norm Bartley, ST 143
L02: Steve Norman, ST 145

When you start the test, please repeat your name and section, and add your U of C ID number at the bottom of the last page.

SCHULICH School of Engineering
UNIVERSITY OF CALGARY

DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING

ENEL 353: Digital Circuits

Midterm Examination

Wednesday, October 25, 2017

Instructions:

- Time allowed is 90 minutes.
- In order to minimize distraction to your fellow students, you may not leave during the last 10 minutes of the examination.
- The examination is closed-book.
- You may use one of the following sanctioned Schulich School of Engineering calculators: Casio FX-260, Casio FX-300MS, TI- 30XIIS.
- The maximum number of marks is 50, as indicated; the midterm examination counts 20% toward the final grade.
- Please use a pen or heavy pencil to ensure legibility.
- Please answer questions in the spaces provided; if space is insufficient, please use the back of the pages.
- Please show your work; where appropriate, marks will be awarded for proper and well-reasoned explanations.

1. Questions about encodings of numbers. **[10 marks total.]**

   (a) **[1 mark.]** What is the value of $31D_{16}$ as a decimal number?

   (b) **[2 marks.]** Use repeated division to convert 1515_{10} to octal representation.

   (c) **[2 marks.]** Convert $F5B2_{16}$ to octal representation.

   (d) **[3 marks.]** Consider the 8-bit pattern 10001001_2. What decimal number does it represent in an unsigned binary system?

   What decimal number does it represent in a 8-bit two's-complement system?

   What decimal number does it represent in a 8-bit sign/magnitude system?

   (e) **[2 marks.]** Complete the table of conversions from 4-bit unsigned binary to Gray code. (Hint: There is a much faster method than doing 12 separate binary-to-Gray conversions!)

unsigned binary	Gray code	unsigned binary	Gray code
0000	0000	1000	
0001	0001	1001	
0010	0011	1010	
0011	0010	1011	
0100		1100	
0101		1101	
0110		1110	
0111		1111	

2. **[5 marks total.]** Questions about binary integer addition.

   (a) **[2 marks.]** Consider this 12-bit binary addition:

carries:	1	1101 1010 0000
a:		0110 1101 0100
b:		1010 0101 0011
sum:		0001 0010 0111

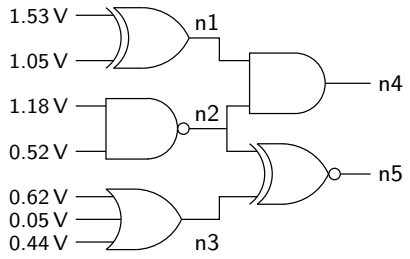
   If a, b and the sum are all interpreted as two's-complement numbers, is there overflow in the addition? Give a reason for your answer.

   If a, b and the sum are all interpreted as unsigned numbers, is there overflow in the addition? Give a reason for your answer.

   (b) **[3 marks.]** Bit patterns 0110_2 and 1101_2 are supplied as inputs to a 4-bit binary adder circuit. What are the values of the sum and overall carry-out? (Give both answers as sequences of one or more bits.)

3. **[3 marks.]** The table below shows some voltage specifications for the Advanced Ultra-Low-Voltage CMOS logic family using a the power supply voltage of 1.80 V.

parameter	voltage
V_{IH}	1.17 V
V_{IL}	0.63 V
V_{OH}	1.20 V
V_{OL}	0.45 V



   Give ranges of voltages that are as precise as possible for nodes n1, n2, n3, n4, and n5. If for some node(s) it is not possible to give a range of voltages, give a reason for that.

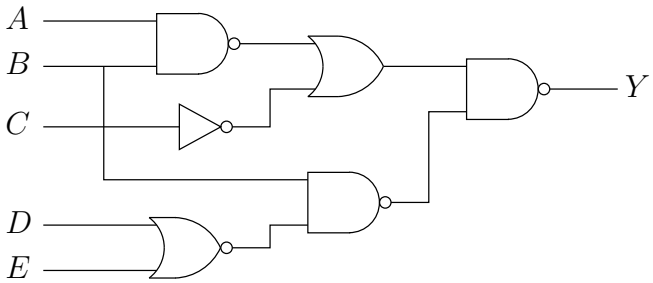
4. **[6 marks.]** Consider the Boolean expression below:

$$Y = \overline{A}C\overline{D} + \overline{C}D + ABD + ABC\overline{D} + B\overline{C}D + \overline{A}\,\overline{C}\,\overline{D}.$$

Use *algebraic manipulation* to simplify Y to a minimal SOP form having three product terms and seven literals. You do not have to give names and numbers for theorems you use along the way, but you must clearly show all your steps. *(Do not use a K-map.)*

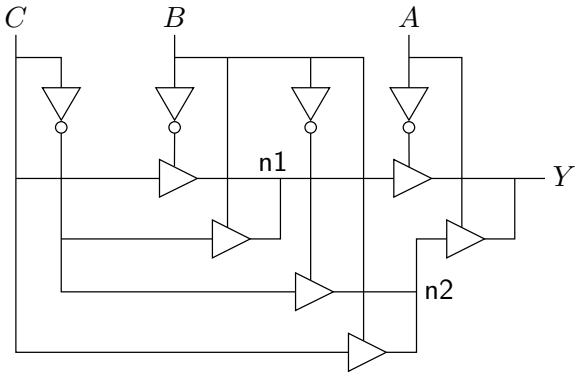
5. **[6 marks total.]** Questions about combinational circuits.

   (a) **[3 marks.]** Consider this circuit:



   Use "bubble-pushing" and/or Boolean algebra to find an SOP expression for Y as a function of A, B, C, D, and E.

   (b) **[3 marks.]** Consider the circuit below, and find a canonical SOP expression for Y as a function of A, B, and C.

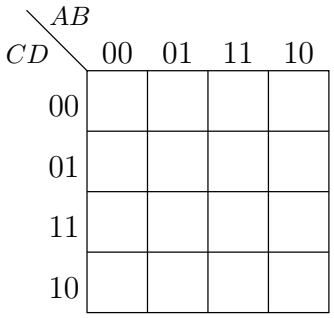


6. **[11 marks total.]** Questions on K-maps and minimal forms.

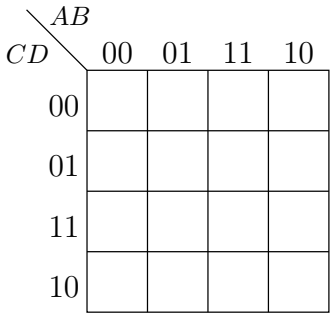
   (a) **[9 marks.]** Consider the function Y given in the truth table below. Use the first K-map to derive all minimal SOP expressions for Y, then use the second blank K-map to derive *all* minimum SOP expressions for Y. You may add more maps if you need them.

A	B	C	D	Y
0	0	0	0	0
0	0	0	1	0
0	0	1	0	X
0	0	1	1	0
0	1	0	0	1
0	1	0	1	0
0	1	1	0	1
0	1	1	1	0
1	0	0	0	0
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	X
1	1	0	1	1
1	1	1	0	0
1	1	1	1	X

Find all minimal SOP expressions



Find all minimal POS expressions



   (b) **[2 marks.]** Sketch a two-level NAND-NAND circuit implementation for one of your answers in part (a). Assume that A, B, C and D are available in true and complementary forms. There is no restriction on the number of inputs on each gate.

7. [**4 marks.**] For the function described by the truth table ...

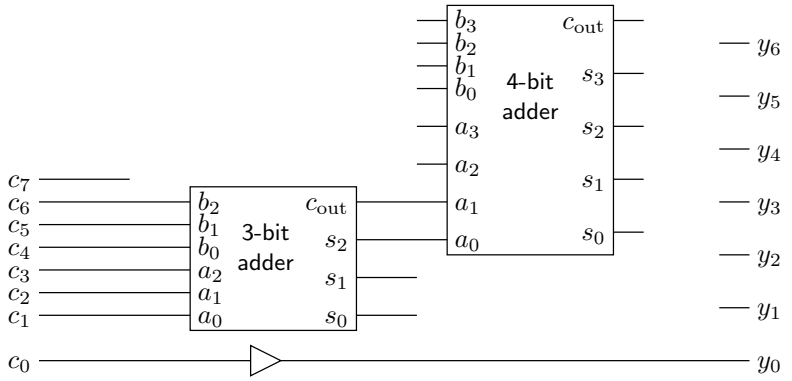
A	B	C	$F(A,B,C)$
0	0	0	1
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1

List all the implicants ...

List all the prime implicants ...

List all the essential prime implicants ...

8. [**5 marks.**] Consider the problem of converting an 8-bit BCD representation of an integer to a 7-bit unsigned binary representation of the same integer. Suppose that $c_7\,c_6\,c_5\,c_4\;\;c_3\,c_2\,c_1\,c_0$ are the BCD bits and $y_6\,y_5\,y_4\,y_3\,y_2\,y_1\,y_0$ are the unsigned binary bits. The following incomplete schematic is the beginning of a design that uses a 3-bit binary adder and a 4-bit binary adder to do the conversion. Add wires so that the circuit will perform the specified conversion.



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Q 1	Q 2	Q 3	Q 4	Q 5	Q 6	Q 7	Q 8	TOTAL
/10	/5	/3	/6	/6	/11	/4	/5	/ 50