University of Calgary
ENEL 353 - Digital Circuits
Midterm Examination – Monday, October 26, 5:00 PM, 2020

Instructions

- **Due Date and Time:** The completed exam is due on Tuesday, October 27 at 5:00 PM.
- **Open-book exam:** You may refer to any books, notes, or websites you choose while writing the exam, except that you may not use websites to communicate with other people about the exam.
- **Use of electronics:** All desktop and laptop computers, tablets, smartphones and calculators are allowed, and all software applications are allowed, except that none of these these devices may be used to communicate with other people about the exam.
- **Individual effort and academic integrity:** Each student is expected to hand in work that is entirely their own. If there is strong evidence that a student has received help from another person (other than a clarification from one of the course lecture instructors) during the course of the exam, that student will be reported for suspected academic misconduct.
- **Submission of PDF files to D2L Dropboxes.**
  - In order to facilitate marking, this exam has been split into Component One, Component Two and Component Three. You must upload three PDF files: one for each component.
  - It is your responsibility to ensure that the PDF files are easy to read and complete. For convenience, you may print out the question paper and write your answers directly in blank spaces provided. You may add extra paper if you need it.
  - The dropboxes are configured to allow you to **replace** a submission as many times as you like before the deadline. Please keep in mind that this implies that you must resubmit **all answers for a component** to the dropbox even if you are only changing the answer to one problem.
- Be sure to write your name, tutorial section, and ID number on all three components of your exam.
- The maximum number of marks is 53. Please show your work!

Component One

Name: _____ *Lecture Section:* _____

L01 — N. Bartley
L02 — S. Norman

1. **[Total of 11 marks.]** In parts (a), (b) and (c) you must show your work carefully to get credit.

   (a) **[3 marks.]** Use repeated division to convert 5095_{10} to hexadecimal representation.

   (b) **[2 marks.]** Find the octal representation of $\mathrm{E5BC}_{16}$.

   (c) **[2 marks.]** What is the decimal representation of the 8-bit two's complement number 11101011?

   (d) **[2 marks.]** Complete the following 6-bit integer addition. Show all of the carry bits involved regardless of whether they are 0's or 1's.

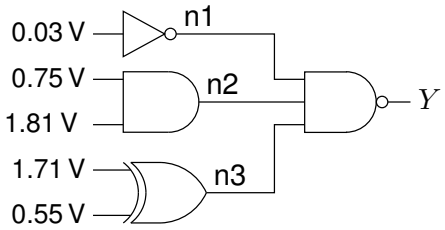
$$\begin{array}{cccccccc} & & 1 & 1 & 0 & 0 & 1 & 1 \\ + & & 0 & 1 & 1 & 0 & 1 & 0 \\ \hline \end{array}$$

   (e) **[1 marks.]** If all the integers in part (d) are interpreted as two's complement, is there overflow in the addition? Give a reason for your answer.

   (f) **[1 marks.]** If all the integers in part (d) are interpreted as unsigned, is there overflow in the addition? Give a reason for your answer.

2. [**4 marks.**] The table below gives voltage parameters for Advanced Ultra-Low-Voltage CMOS logic gates operating with V_{DD} equal to 2.50 V. For each of nodes n1, n2, n3 and Y in the circuit below, either state the range of possible output voltages or give a reason why a range cannot be determined.

parameter	voltage
V_{IH}	1.70 V
V_{IL}	0.70 V
V_{OH}	1.80 V
V_{OL}	0.60 V



3. [**Total of 4 marks.**]

   (a) [**3 marks.**] Find a canonical product-of-sums expression for the function given by the truth table.

A	B	C	D	Y
0	0	0	0	0
0	0	0	1	1
0	0	1	0	1
0	0	1	1	1
0	1	0	0	1
0	1	0	1	1
0	1	1	0	0
0	1	1	1	1
1	0	0	0	1
1	0	0	1	1
1	0	1	0	0
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0

   (b) [**1 mark.**] How many products would there be in a canonical sum-of-products expression for the function? (You do *not* have to list all the products.)

Component Two

Name: _____ *Lecture Section:* _____

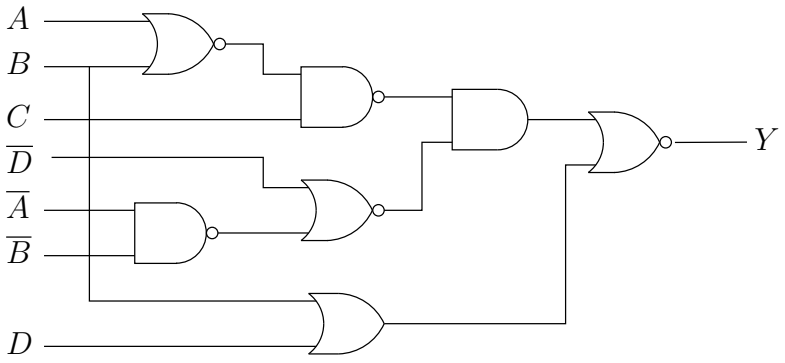
L01 — N. Bartley
L02 — S. Norman

4. **[Total of 8 marks.]**

(a) **[4 marks.]** Use algebraic manipulation to simplify Y in the following expression to a minimal SOP form having three product terms and five literals. (You may check your work with a truth table or a K-map, but you must not include any truth table or K-map work as part of your answer.)

$$Y = A \oplus B \oplus C + (\overline{A \oplus B})C$$

(b) **[4 marks.]** Consider the schematic below. Use "bubble-pushing" and/or Boolean algebra to find an SOP expression for the function Y.

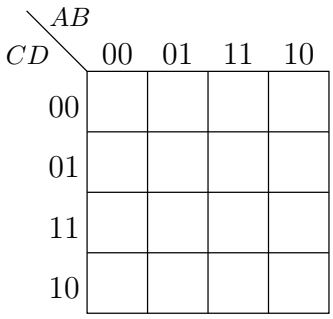


5. [**Total of 10 marks.**]

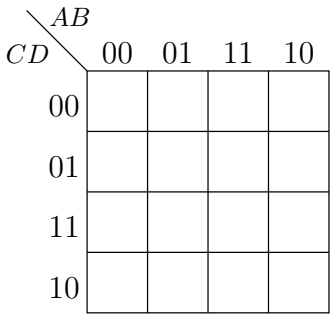
(a) **[5 marks.]** Consider the function

$$Y(A,B,C,D) = \sum(0,1,2,5,7,9) + X(A,B,C,D),$$

where $X(A,B,C,D) = \sum(6,8,11,13,14,15)$ are don't-cares. Derive *all* possible minimal SOP expressions for Y.



(b) **[5 marks.]** Derive *all* possible minimal POS expressions for Y in part (a). Indicate all distinguished 1-cells and essential prime implicants.



Component Three

Name: _____ *Lecture Section:* _____

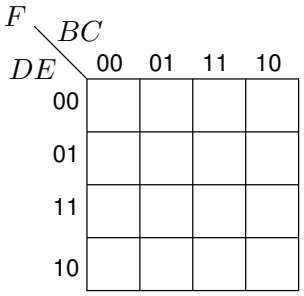
L01 — N. Bartley
L02 — S. Norman

6. **[5 marks.]**

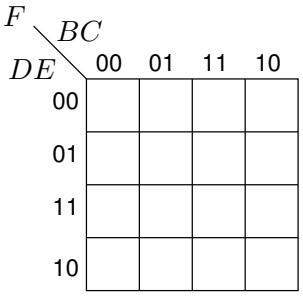
The truth table for function $F(A, B, C, D, E)$ can be described as follows:

- output is 1 in rows 1, 2, 3, 9, 11, 13, 15, 16, 17, 18, 19
- output is 0 in rows 0, 4, 5, 6, 7, 8, 10, 12, 14, 20, 21, 22, 23
- output is don't-care in rows 24–31

Fill in the following 5-variable K-map, and then use it to find a minimal SOP expression for F. If there is more than one such expression, you only need to give one of them.



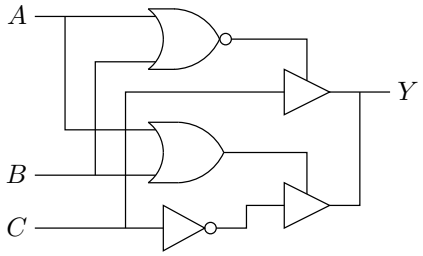
$A = 0$



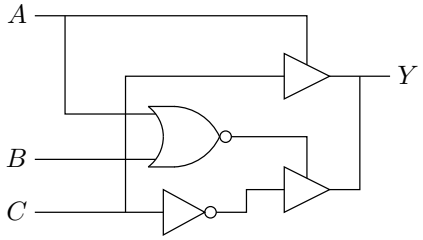
$A = 1$

7. [**Total of 4 marks.**]

   (a) **[2 marks.]** Either give an SOP expression for Y as a function of A, B and C, or explain why it is not possible to do so.

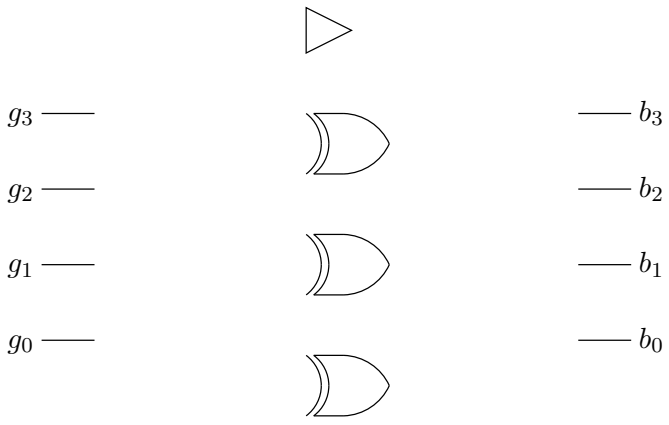


   (b) **[2 marks.]** Either give an SOP expression for Y as a function of A, B and C, or explain why it is not possible to do so.



8. **[3 marks.]** Add wires but no more gates to make a 4-bit Gray code to unsigned binary converter circuit. $g_3g_2g_1g_0$ is the Gray code and $b_3b_2b_1b_0$ is the unsigned binary number. You must use all four of the given gates.

   To help with readability, please use horizontal and vertical lines only when drawing wires.



9. [**4 marks.**]

Consider the multiplexer circuit below in which A is the most-significant select bit. Derive a SOP expression for $Y(A, B, C, D)$.