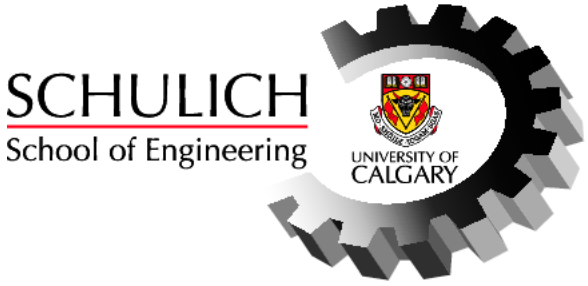
Name or ID: _____ Lecture Section: _____

L01 - Norm Bartley
L02 - Svetlana Yanushkevich



DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING

ENEL 353 - Digital Circuits

Midterm Examination

Wednesday, November 8, 2006
Time: 5:00 - 6:30 PM

Instructions:

- Time allowed is 90 minutes.
- The examination is closed-book.
- Non-programmable calculators are permitted.
- The maximum number of marks is 50, as indicated; the midterm examination counts 15% toward the final grade.
- Please use a pen or heavy pencil to ensure legibility.
- Please answer questions in the spaces provided; if space is insufficient, please use the back of the pages.
- Please show your work; marks will be awarded for proper and well-reasoned explanations.

Name: _____, *ID:* _____

1. **[10 marks total.]**

   (a) **[6 marks.]** Represent the following numbers using 7-bit 2's-complement format and perform the addition. Indicate in each case if an overflow occurs, and why. Convert your answer to signed decimal notation.

      i. 48_{10} + 23_{10}

      ii. 14_{10} + (-33_{10})

   (b) **[2 marks.]** Represent each of the following numbers in 7-bit sign-magnitude and 2's-complement binary formats.

      i. 33_8

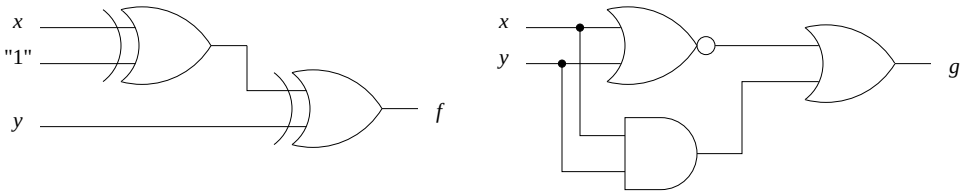
      ii. $(-3E)_{16}$

(c) **[2 marks].** Add the decimal numbers 96 and 87 using BCD arithmetic.

2. **[8 marks total (4 marks each).]** Perform algebraic manipulation for each of the following tasks:

(a) Expand the function $f = a + b + c'$ to its canonical form.

(b) Prove or disprove algebraically that the following circuits are functionally equal:



3. **[6 marks total.]** Karnaugh maps are given identically for a function $F(a, b, c, d)$ in parts (a) and (b) below:

   (a) **[3 marks.]** Find a minimal SOP algebraic expression using this map.

   - If there is more than one minimal sum, give any *one* of them.
   - Give the "cost" associated with this function (give the number of gate-inputs as well as the number of gates, assuming any number of inputs is allowed on each gate).

ab \ *cd*	00	01	11	10
00	1	1	0	1
01	1	1	1	0
11	0	1	1	0
10	0	0	1	1

   (b) **[3 marks.]** Similarly, find any *one* minimal POS expression using this map, and give the "cost" associated with this function.

ab \ *cd*	00	01	11	10
00	1	1	0	1
01	1	1	1	0
11	0	1	1	0
10	0	0	1	1

Note: *When drawing circuits in the questions below, you may assume that the inputs are available in both complemented and uncomplemented form.*

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4. **[18 marks total.]** Consider a two-bit magnitude comparator circuit such as the one designed in Lab #2. It has two two-bit inputs $A = a_1a_0$ and $B = b_1b_0$ (where a_1 and b_1 are the most-significant bits). The output f should be $f = 1$ when $A \neq B$; otherwise $f = 0$.

   (a) **[4 marks.]** Find a minimal SOP expression for f. Draw the logic diagram of an *AND-OR* circuit implementation of f using only 2-input gates. Use whatever answer you obtain here to answer parts (b)-(d) below.

(b) **[4 marks.]** Using algebraic transformations and/or circuit manipulation, implement the circuit you drew in part (a) using 2-input NAND gates only (inverters are not available).

(c) **[4 marks.]** Implement the logic function f using 2-to-4 decoders. You may use any additional AND, OR, and NOT gates as necessary. Each decoder has an ENABLE input.

(d) **[6 marks.]** Implement the logic function f using two 4-to-1 muliplexers and one 2-to-1 multiplexer. You may use any additional AND, OR, and NOT gates as necessary.

5. **[8 marks.]** Design a circuit with four inputs x_3, x_2, x_1, x_0 (x_3 is the MSB) and two outputs f_1 and f_2 that implements a BCD code detector. The function f_1 should be $f_1 = 1$ if the BCD code is 1, 3, 5 or 7; otherwise $f_1 = 0$. The function f_2 should be $f_2 = 1$ if the code is 0, 5, 6, 7 or 8; otherwise $f_2 = 0$.

   Give minimal SOP expressions for each output suitable for the simplest-possible multiple-output circuit implementation. Use don't-cares for the invalid BCD codes. Carefully indicate shared product terms (if any) that can be used. (It is not necessary to draw the circuit.)