Name: _____

Lecture Section: _____
L01 – A 140, 11:00-11:50
L02 – SA 104, 12:00-12:50

SCHULICH School of Engineering
UNIVERSITY OF CALGARY

DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING

ENEL 353 - Digital Circuits

Midterm Examination

Thusday, November 3, 2011

Instructions:

- Time allowed is 90 minutes.
- The examination is closed-book.
- Non-programmable calculators are permitted.
- The maximum number of marks is 50, as indicated; the midterm examination counts 15% toward the final grade.
- Please use a pen or heavy pencil to ensure legibility.
- Please answer questions in the spaces provided; if space is insufficient, please use the back of the pages.
- Please show your work; where appropriate, marks will be awarded for proper and well-reasoned explanations.

UCID: _____

1. **[12 marks total.]**

   (a) **[6 marks.]** Represent the numbers below using 7-bit 2's-complement format and perform the addition. Indicate in each case if an overflow occurs, and why. Convert your answer to signed decimal notation.

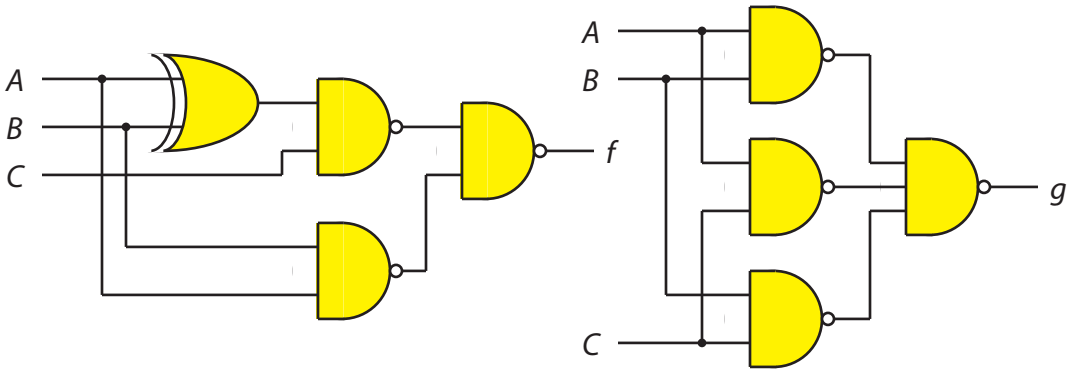
      i. $-64_{10} + 43_{10}$

      ii. $29_{10} + 43_{10}$

   (b) **[3 marks.]** Let $A = 110110_2$ and $B = 001110_2$. Each are 6-bit numbers in *sign-magnitude* format. Determine $A + B$, and give your answer in 6-bit sign-magnitude format.

(c) **[3 marks.]** Convert the decimal numbers 89_{10} and 84_{10} into Binary-Coded Decimal (BCD) format and perform BCD addition.

2. **[10 marks total.]** Consider the two circuits below.



(a) **[5 marks.]** By *algebraic manipulation*, prove or disprove that $f = g$ in the two circuits. (Do not use a truth table.)

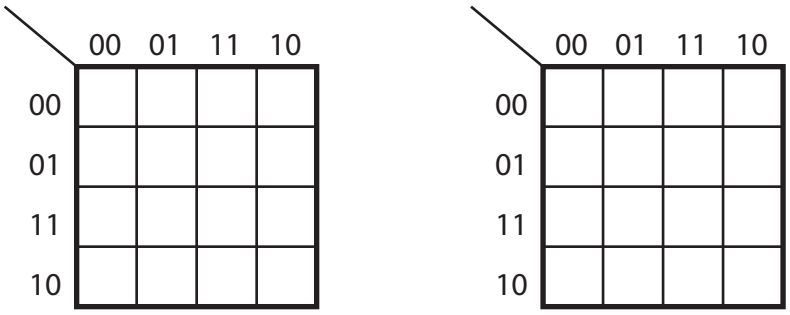
BONUS! [+1 mark]: *What important application does the circuit for g serve?*

(b) **[5 marks.]** Using any method you wish, sketch the *simplest-possible* circuit for g based only on NOR gates. For convenience, inverters are available, and NOR gates with any number of inputs may be used. Inputs are available in both complemented and uncomplemented form.

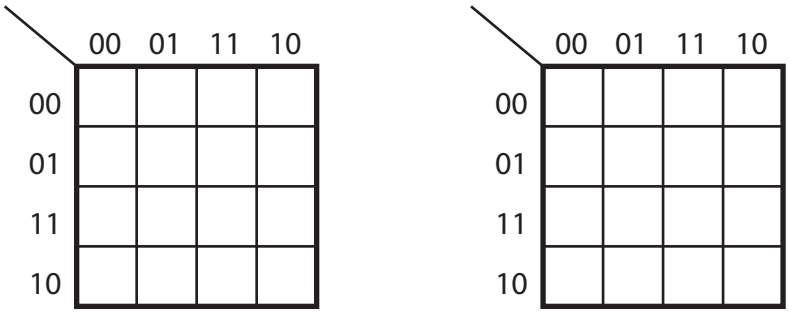
3. **[20 marks total.]** Consider the function f given by

$$f(a,b,c,d) = \sum m(4,10,11,12,14) + \sum d(1,3,5,8,9). \tag{1}$$

(a) **[3 marks.]** Identically fill in the two empty K-maps below for f, and find two minimal *POS* expressions.

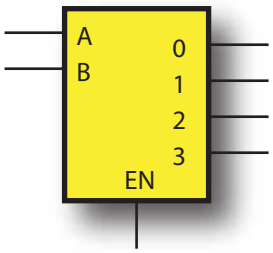


(b) **[5 marks.]** Now find four minimal *SOP* expressions for f using the empty K-maps below. (Please use the back of the pages if you need to draw more maps.)



(c) **[5 marks.]** Sketch a two-level AND-OR circuit based on any one of your four SOP expression in part (b), and then sketch the circuit using *two-input NOR* gates only. Inputs are available in both complemented and uncomplemented form, but you will need to create inverters using NAND gates if needed.

(d) **[4 marks.]** Using generic 2-to-4 decoders of the type shown below, plus any other gates you may need, implement the function f' (i.e., the complement of equation (1)). The A input of the decoder is the MSB (Most-Significant Bit).



(e) **[3 marks.]** Now, consider the function g given by

$$g(a,b,c,d) = \sum m(0,3,8,11) + \sum d(4,7,12,15). \tag{2}$$

Try to implement this function with *just one* generic 2-to-4 decoder and any other gates you may need.

4. **[8 marks.]** Give SOP expressions for each of the functions below corresponding to the lowest-cost *overall* circuit implementation (i.e., an overall implementation with the smallest-possible number of gates and gate inputs). Carefully indicate shared product terms (if any) that can be used, and calculate the overall cost. *(It is not necessary to draw the circuit.)*

   - *Map for F:*

cd \ ab	00	01	11	10
00		1	1	1
01		1	1	1
11			1	
10	1		1	1

   - *Map for G:*

cd \ ab	00	01	11	10
00				1
01	1			1
11	1		1	1
10	1			

   - *Map for H:*

cd \ ab	00	01	11	10
00		1	1	
01	1	1	1	1
11			1	
10	1			