Exam Review Problems

for ENEL 353 Fall 2019 Section 02

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Outline of Exam Review Problems

A sequence detection problem

From the 2013 final exam . . .

Consider the design of a Moore-type FSM that has one input A and one output Y.

Y should be 1 if the values of A at the last 5 rising edges of the clock have been 1, 1, 0, 1, 1.

Y should be 0 at all other times.

Part a. Choose states for an FSM design, and describe them in the table below. (If you need fewer than eight states, write "unused" beside the names of states you don't use.) Then make a **state-transition diagram** for the FSM.

state	**description**
S0	*from reset, or looking for first 1 in 11011*
S1	
S2	
S3	
S4	
S5	
S6	
S7	

Part b. Instead of going on to make tables for next-state and output logic, consider a totally different method of implementation.

Draw a schematic for the sequence detector, using
5 D flip-flops in a shift register configuration, one NOR gate with however many inputs you need, and some inverters.

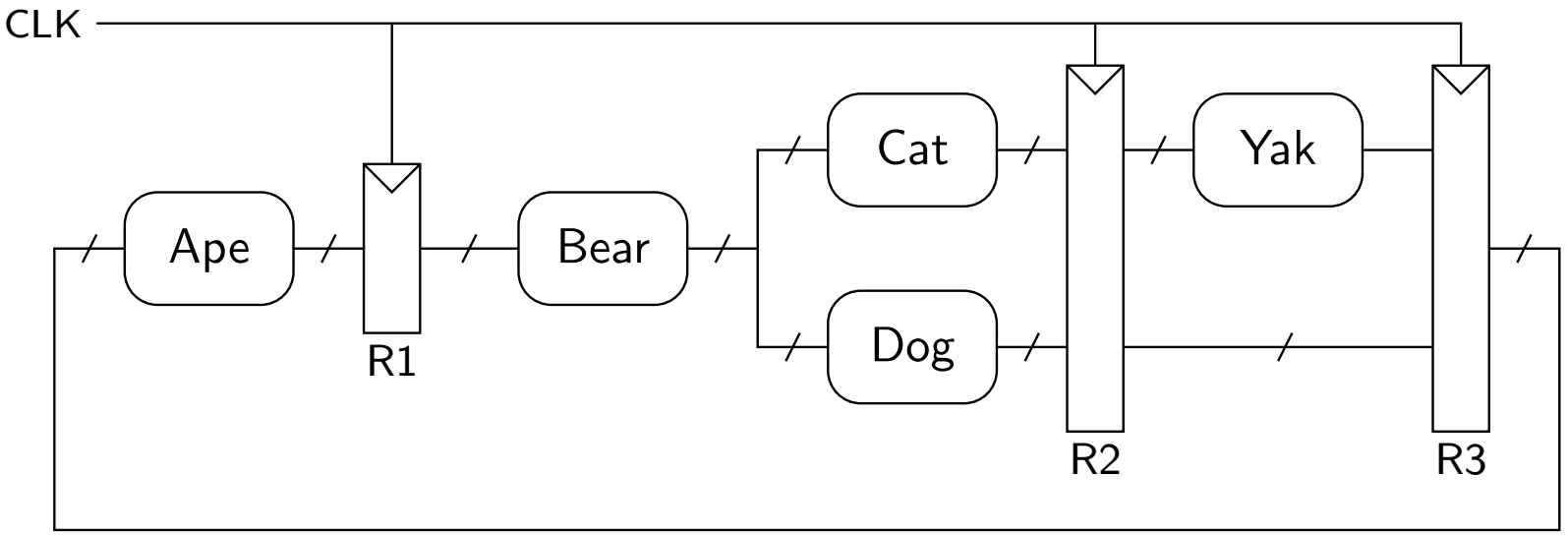
(This shift-register part of this problem would not be a fair exam question in 2019.)

Outline of Exam Review Problems

A synchronous logic timing problem

This is from the quiz of December 1, 2015.

The circuit below is built with five combinational elements and three registers.



The clock period is $T_c = 320\,\text{ps}$. The timing parameters for all three registers are: $t_{\text{setup}} = 40\,\text{ps}$, $t_{\text{hold}} = 15\,\text{ps}$, $t_{\text{pcq}} = 55\,\text{ps}$, and $t_{\text{ccq}} = 27\,\text{ps}$.

Here are the timing parameters for the combinational logic, with all values in ps:

element	t_{pd}	t_{cd}
Ape	200	50
Bear	60	30
Cat	100	40
Dog	80	35
Yak	190	60

Part a. Suppose that the design team wants to replace Dog with a different component that is slower but uses less energy. What is the maximum allowable t_{pd} for this replacement for Dog? Assume that there is some clock skew, with $t_{skew} = 20\,\text{ps}$.

Extension to part a. Let's confirm that **all** parts of the system meet the setup-time constraint.

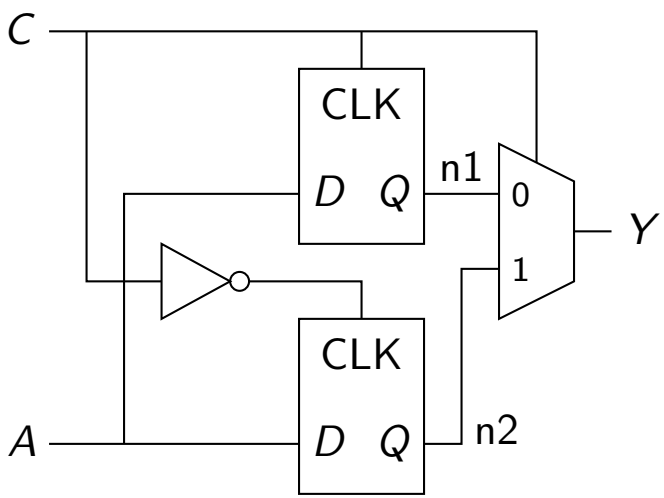
Part b. Contrary to **part a**, now assume that t_{skew} is unknown, because the design team is considering changes to the wires that deliver CLK to the registers. How large can t_{skew} be without causing a hold-time violation anywhere in the circuit?

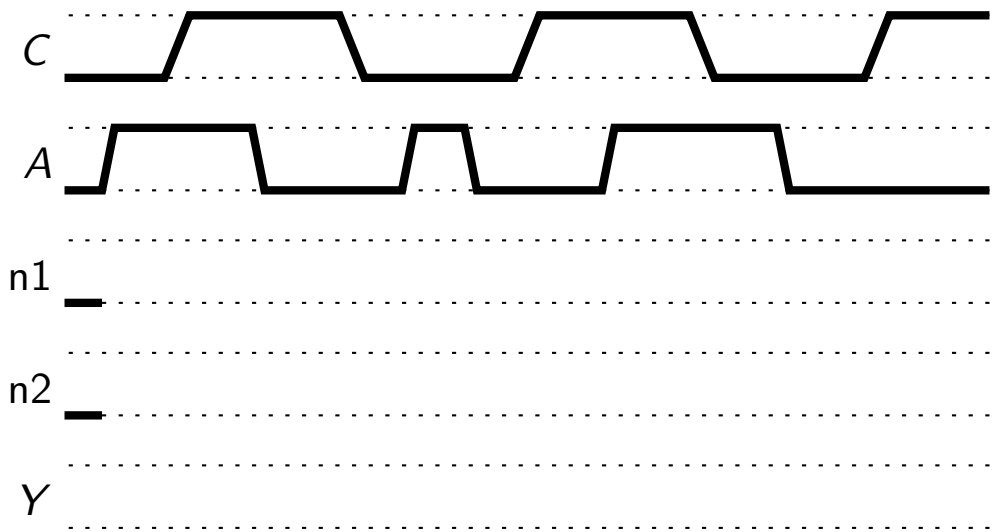
Extension to part b. What modification could be made to the circuit to maintain its functionality, while being tolerant of up to 20 ps of clock skew?

Outline of Exam Review Problems

Question 4 (b) from Fall 2014 exam

The schematic below shows a circuit built with two D latches, an inverter, and a 2:1 mux. Complete the timing diagram.





Outline of Exam Review Problems

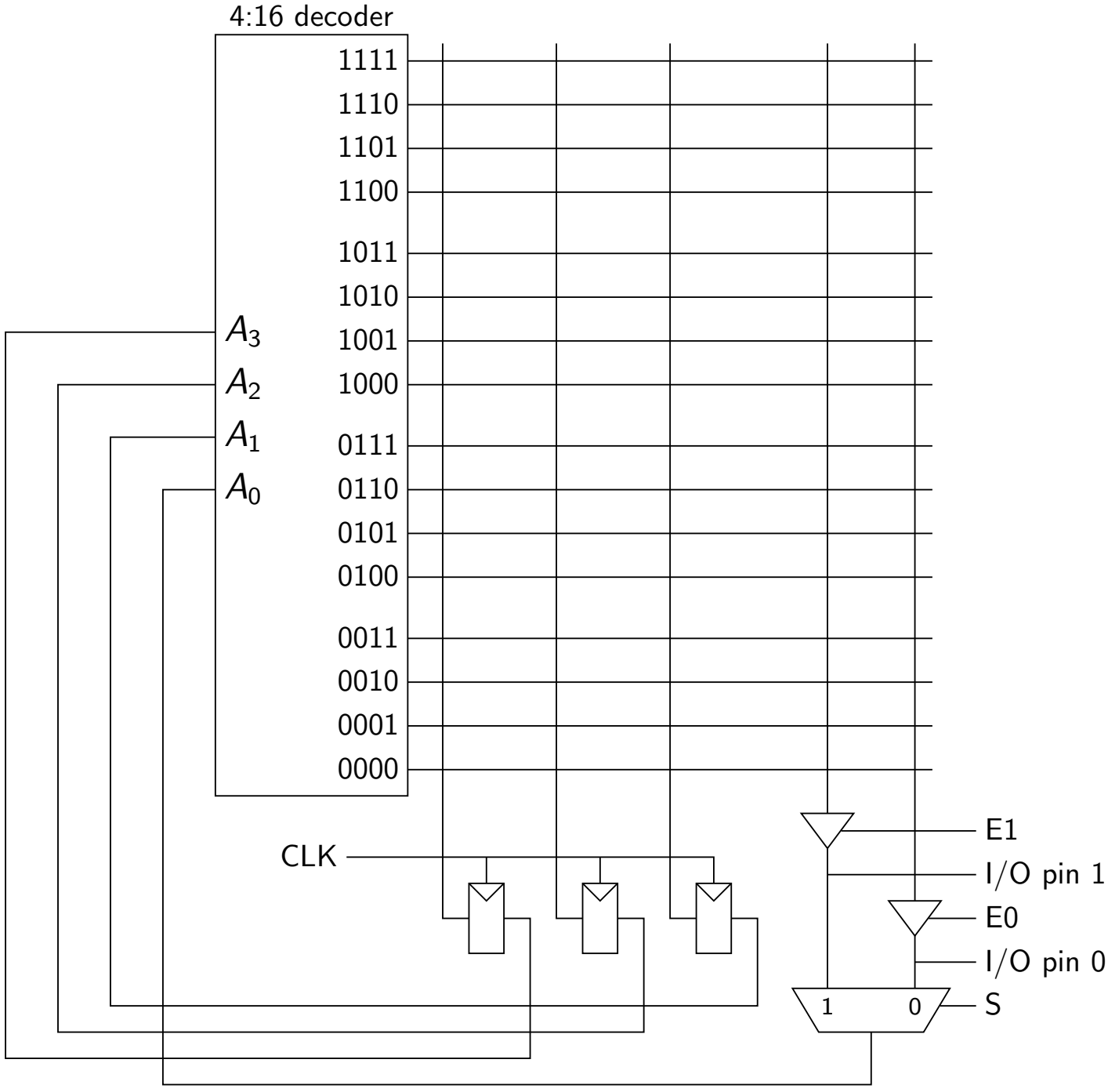
Question 6 from Fall 2014 exam

This problem has been edited a little to make it fit into a sequence of slides!

An engineer has designed a Moore-type FSM. Using $Q_{2:0}$ for the state and B as the name of the 1-bit input, next-state and output equations are:

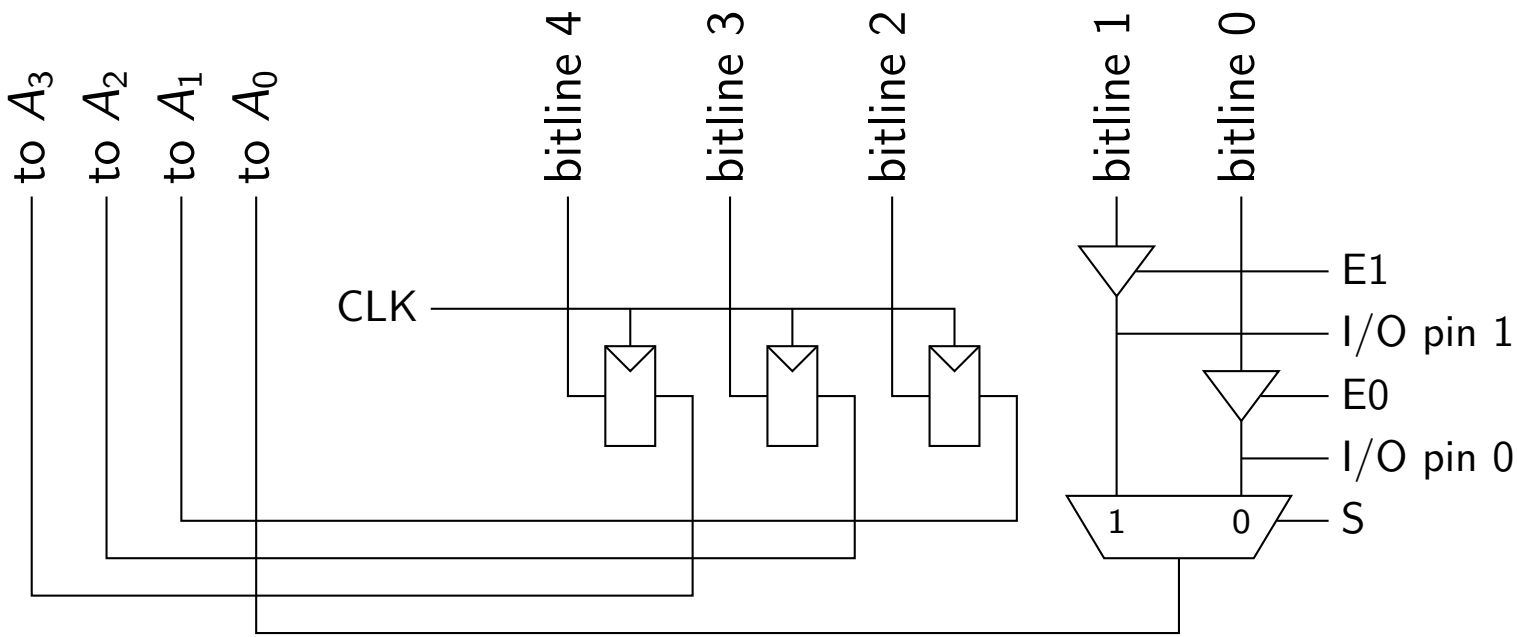
$$
\begin{aligned}
Q_2' &= Q_2\,\overline{Q_1}\,\overline{Q_0} + Q_2\,\overline{Q_1}\,B + Q_1\,Q_0\,\overline{B} \\
Q_1' &= Q_1\,\overline{Q_0} + \overline{Q_1}\,Q_0\,B \\
Q_0' &= Q_1\,\overline{Q_0}\,\overline{B} + \overline{Q_1}\,\overline{Q_0}\,B + Q_1\,Q_0\,B \\
Y &= Q_2\,Q_1\,\overline{Q_0}
\end{aligned}
$$

The FSM will be implemented using a ROM array and a few other components that should be familiar to you. The circuit is shown on the next slide . . .


4:16 decoder
1111
1110
1101
1100
1011
1010
1001
1000
0111
0110
0101
0100
0011
0010
0001
0000
A_3
A_2
A_1
A_0
CLK
E1
I/O pin 1
E0
I/O pin 0
1
0
S

Part a. A decision has been made to use I/O pin 0 for B and I/O pin 1 for Y. Fill in the table to specify and explain the correct values for the tristate enable signals E1 and E0 and the mux select signal S.

signal	0 or 1?	reason
E1		
E0		
S		



Part b. Use dot notation on the given ROM array to show how to implement the next-state and output logic for the FSM. *Use the space above and beside the schematic to show any work you need to do to decide where to place dots.*

Outline of Exam Review Problems

Question 8 (c) from Fall 2014 exam

Part (c) of this question was dependent on the solution to part (a), which is shown on the next slide.

Part (c) asks: Draw a state-transition diagram for a *Moore-type* FSM that mimics the Mealy-type FSM of part (a) as closely as possible. Hypothetically, for example, if the Mealy output is 1 when the current input is 0 and the input has been 0 at the last three rising edges of CLK, then the Moore output should be 1 when the input has been 0 at the last four rising edges of CLK.

[4 marks.] Below is the combined state and output table for a Mealy-type FSM that has one input A, and one output Y. The state variables are $S_{2:0}$. Use the information in this table to sketch a state-transition diagram.

$S_{2:0}$	A	$S'_{2:0}$	Y	$S_{2:0}$	A	$S'_{2:0}$	Y
000	0	001	0	010	1	011	1
000	1	000	0	011	0	001	0
001	0	010	0	011	1	100	0
001	1	000	0	100	0	001	1
010	0	010	0	100	1	000	0