ENEL 353 Section 02 Lecture

Mon Dec 2

Tutorial problems tomorrow

- synchronous system timing
- memory arrays

Lectures this week

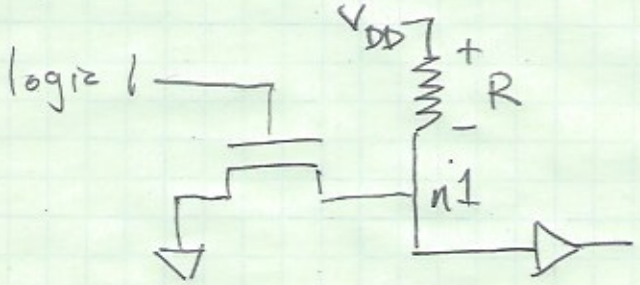
Mon - slide set 10

Wed - finish slide set 10, exam review

Fri - more exam review

Set 10, Slide 37

Let's first do an example with one NMOS transistor connected to a wire - the wire will play the role of a bitline in the ROM circuit.



- current can flow through R
- voltage drop across R close to V_{DD}
- voltage at n1 close to ground
- buffer output is logic 0

In the 4x3 array, if wordline 2 is ON and the other three wordlines are OFF ...

Bitline 2 is HIGH - no transistor is pulling it down.

Bitline 1 is LOW - the NMOS transistor has much lower effective resistance than R, so the voltage drop across R is close to V_{DD}.

Bitline 0 is LOW for the same reason that Bitline 1 is LOW.

Array contents	Address	Data
	11	010
	10	100
	01	110
	00	011

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