ENEL 353 Section 02 Lecture

Wed Dec 4 2019

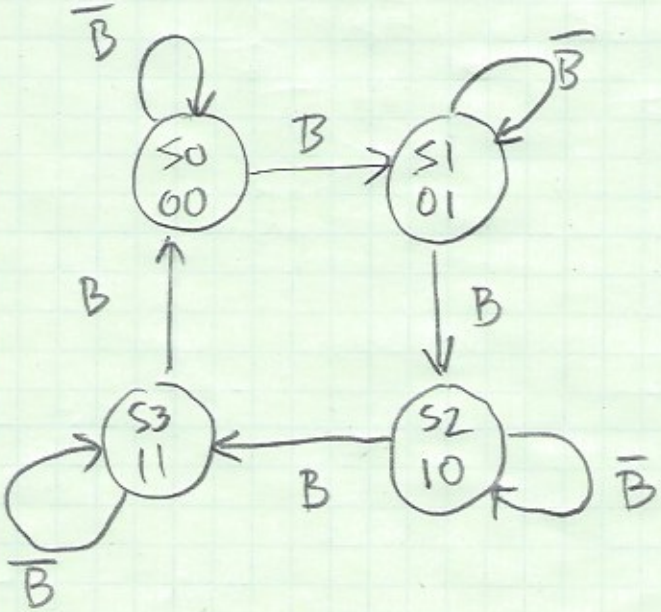
today - finish yesterday's tutorial
- shift registers (not an exam topic)
- PLAs (also not an exam topic)
- exam review

Friday - more exam review

Quiz 4
- about 80 papers have been marked
- about 40 papers have not yet been marked - they will be available Friday

Exercise 5 from yesterday's tutorial

state transition diagram



The output is the state, so the encoding must be

S0	00
S1	01
S2	10
S3	11

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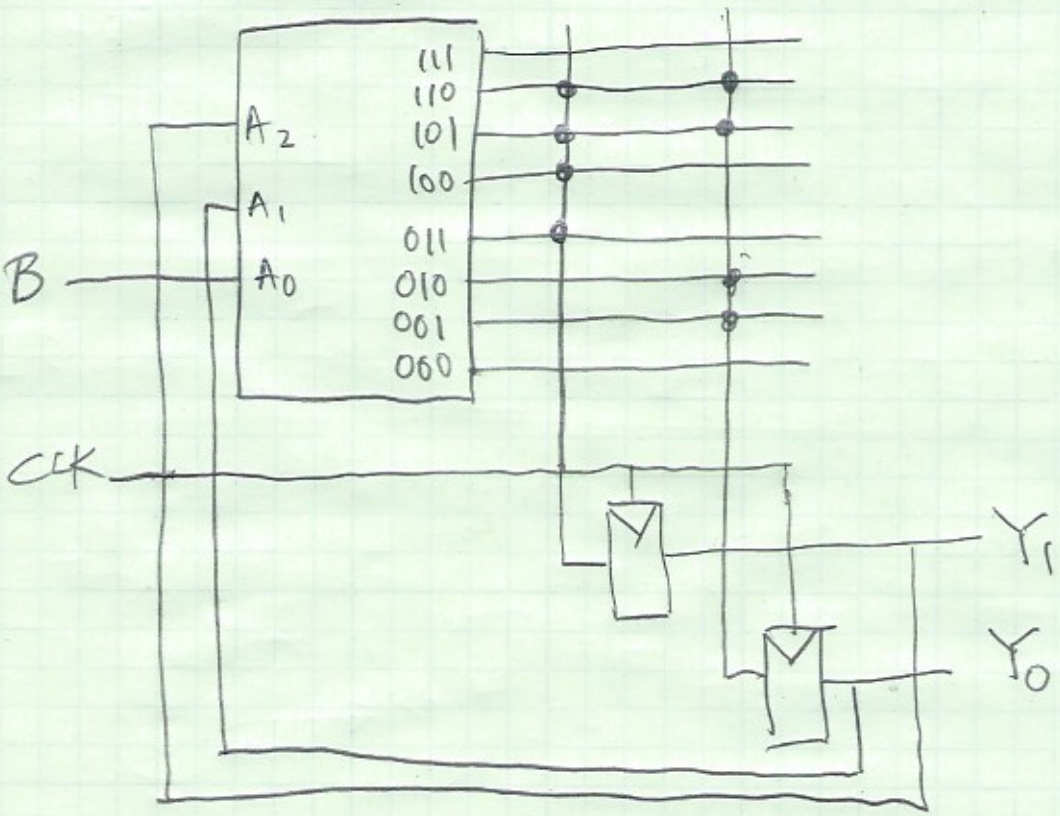
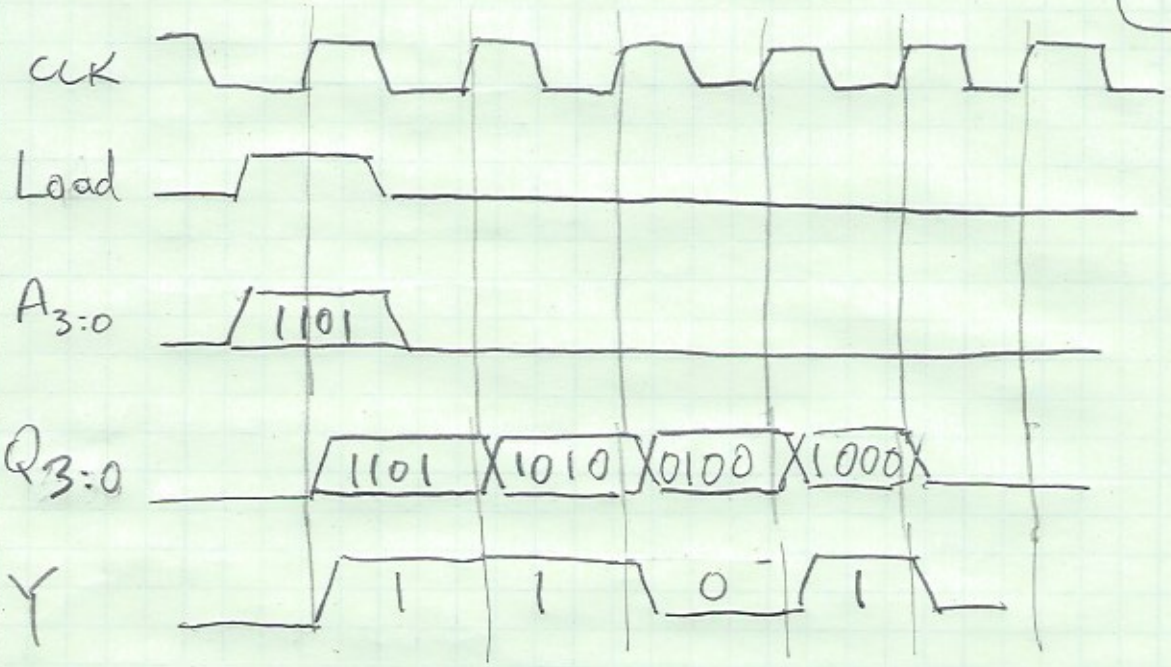
state transition table

Y_1	Y_0	B	Y_1'	Y_0'
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	1	0
1	0	1	1	1
1	1	0	1	1
1	1	1	0	0

3:8 decoder



Set 10, Slide 12



Slide 13

Companion circuit? A counter - for example the counter could count down from 7 down to 0.

Slide 14 For the circuit to work correctly, A must go 1→0 or 0→1 no more than once per clock cycle. Transitions of A must not happen in the DFF setup/hold aperature around rising clock edges.

A special circuit called a "clock recovery circuit" can inspect a signal like A, and produce an appropriate CLK signal.

Exam Review Problem – Sequence detection

Part a.

state	description
S0	from reset, or looking for 1st 1 in 11011
S1	got first 1 in 11011
S2	" 2nd 1 in 11011
S3	got middle 0 in 11011
S4	got 3rd 1 in 11011
S5	got 4th 1 in 11011
S6	unused
S7	unused