ENEL 353 Section 02 Lecture

Wed Nov 6 2019

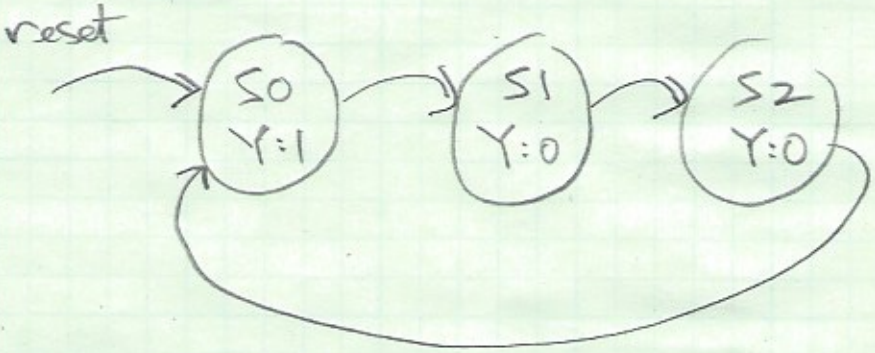
Midterm return – Fri Nov 8

Section B03 Lab 3 reports are due Wed Nov 20.

Set 8, Slide 27

Please do the reading!

Slide 34



Slide 36

state encoding

state	S_1	S_0
S_0	0	0
S_1	0	1
S_2	1	0

state transition table (with state encodings plugged in)

state		next state	
S_1	S_0	S_1'	S_0'
0	0	0	1
0	1	1	0
1	0	0	0
1	1	X	X ← don't-care outputs

next-state equations

S_1'

S_1 \ S_0	0	1
0		
1	1	X

$S_1' = S_0$

S_0'

S_1 \ S_0	0	1
0	1	
1		X

$S_0' = \bar{S}_1 \bar{S}_0$

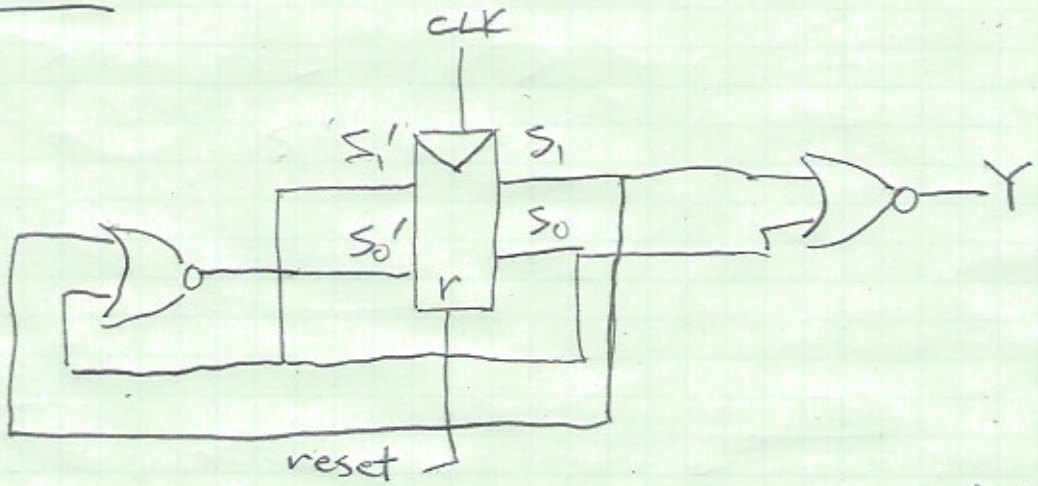
$= NOR(S_1, S_0)$

output logic

S_1	S_0	Y
0	0	1
0	1	0
1	0	0
1	1	X

$Y = \bar{S}_1 \bar{S}_0 = NOR(S_1, S_0)$

schematic



Slide 37 Divide-by-3 counter using one-hot state encoding

state	S_2	S_1	S_0
S0	0	0	1
S1	0	1	0
S2	1	0	0

Remark: There are 5 unused state encodings.

000, 011, 101, 110, 111

State transition table, with state encodings

current state			next state		
S_2	S_1	S_0	S_2'	S_1'	S_0'
0	0	1	0	1	0
0	1	0	1	0	0
1	0	0	0	0	1
[unused states]			x	x	x

next state equations, for the rows that matter

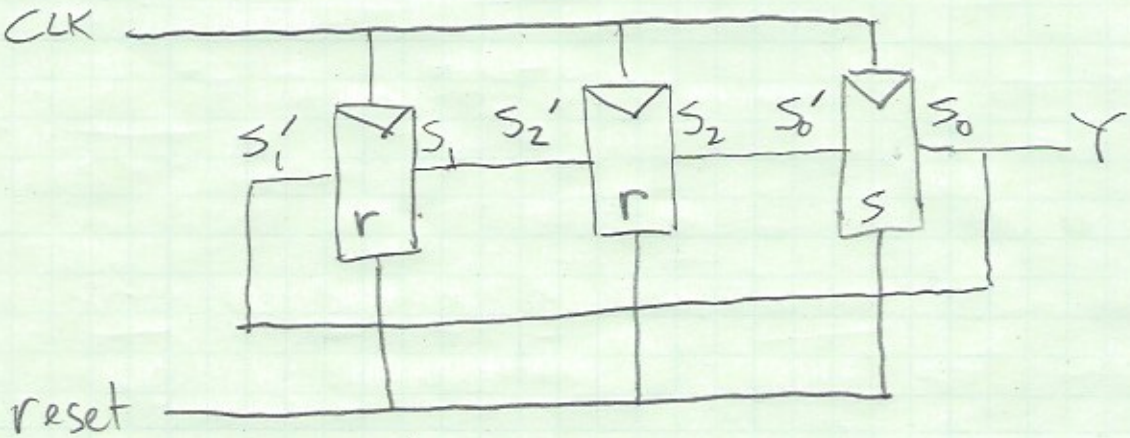
$$S_2' = S_1, \quad S_1' = S_0, \quad S_0' = S_2$$

No logic gates needed! Just wires!

Output logic $Y = S_0$

Reset logic for 1-hot encoding

On reset, the FSM should go to S0, encoded as 001. To make this work, use two resettable DFFs and one settable DFF.



Remark: The structure of this circuit is an example of what is called a shift register.

Slide 41

A: No. Makes a $1 \rightarrow 0$ transition near in time to the rising clock edge at t_3.

B: Yes

C: Two transitions between t_2 and t_3

D: Yes

Slide 42

(a) Moore. Output depends only on current state.

(b) Mealy. Output depends on current state and current input.

Slide 43

Moore: Input was 0 at most recent rising edge of CLK, was 1 at the 3 previous rising edges of CLK.

Mealy: Input was 1 at the 3 most recent rising edges of CLK, current input is 0.