ENEL 353 Section 02 Lecture

Wed Nov 20 2019

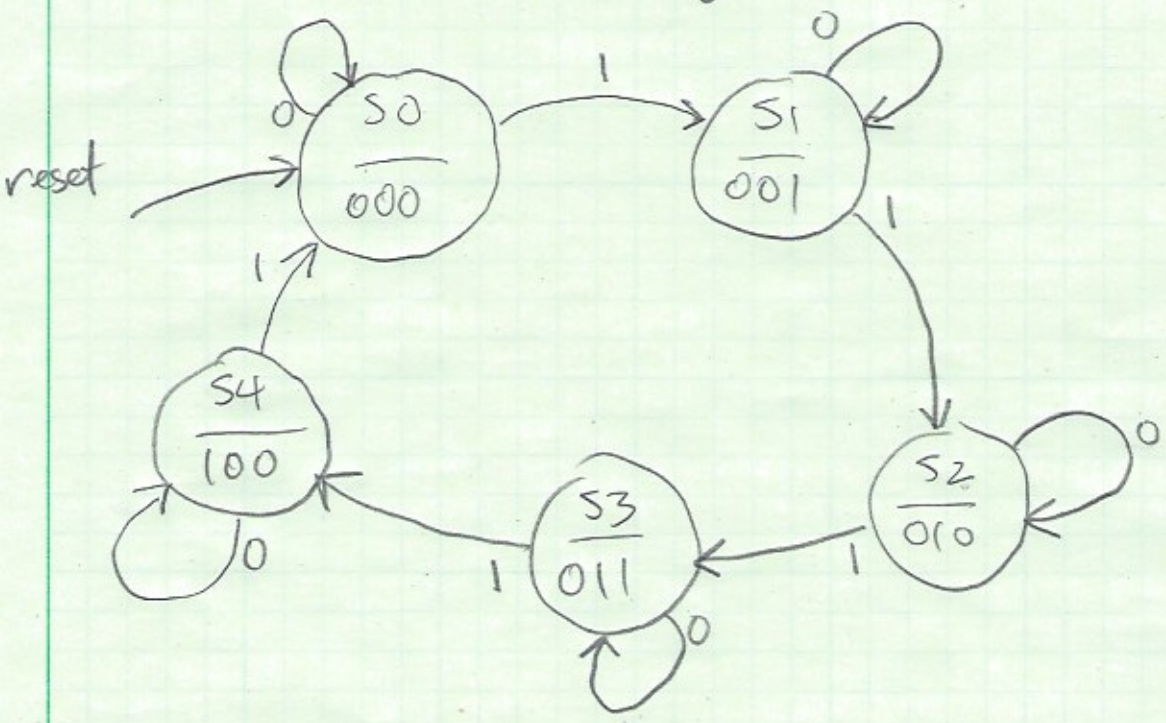
Quiz 4 - Tue Nov 26

- DFF circuits and FSMs
- no questions on Sequential logic timing (t_{pcq}, t_{ccq}, t_{setup}, t_{hold}, etc.)

Quiz 3 return - Fri Nov 22

Set 8, Slide 58 (continued)

State transition diagram



In words ...

On reset, output goes to 000.

If input A=1, count through the sequence 000, 001, 010, 011, 100, 000, 001, ..., updating once per clock cycle.
If A=0, the count is frozen.

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Set 9, Slide 13

- output(s), input(s) – possibly plural for registers made from multiple DFFs
- the input(s) waveform shows a large collection of possible D input signals, all of which satisfy the t_{setup} and t_{hold} conditions.
- the output(s) waveform shows the collection of Q responses to the D inputs
- the earliest possible Q response happens t_{ccq} after the clock edge
- the latest possible Q response happens t_{pcq} after the clock edge