ENEL 353 Section 02 Lecture

Fri Nov 22 2019

Quiz 3 - returned at end of today's lecture
- average was around 16.5/20
- median was 17.5/20
- solutions have been posted

Set 9, Slide 19 - Setup time constraint

D2 must be stable by time $t_0 + T_c - t_{setup}$
In the worst case, D2 is not stable until time $t_0 + t_{pcq} + t_{pd}$. For reliable operation...

$$t_0 + t_{pcq} + t_{pd} \leq t_0 + T_c - t_{setup}$$

$$\boxed{t_{pcq} + t_{pd} \leq T_c - t_{setup}} \quad (*)$$

In a typical design scenario, everything is fixed except t_{pd}. Then inequality (*) says

$$t_{pd} \leq T_c - t_{pcq} - t_{setup}$$

Sometimes t_{pd} is fixed, but there is freedom to choose T_c. Then (*) says

$$T_c \geq t_{pd} + t_{pcq} + t_{setup}$$

Slide 20 – hold time constraint

D2 must be stable at least until time $t_0 + t_{hold}$

D2 might be unstable as-soon as time $t_0 + t_{ccq} + t_{cd}$

For reliable operation,

$$t_0 + t_{hold} \leq t_0 + t_{ccq} + t_{cd}$$

$$\boxed{t_{ccq} + t_{cd} \geq t_{hold}} \quad (**)$$

Remark: Often $t_{hold} = 0$. If not, t_{hold} is usually $\leq t_{ccq}$. In both of these cases, (**) is obviously satisfied. (t_{hold} problems are more likely to occur in the presence of something called clock skew.)

Slide 21

In this case (**) becomes

$$\boxed{t_{ccq} \geq t_{hold}} \quad (***)$$

Remark: Any DFF with $t_{ccq} < t_{hold}$ is a badly-designed DFF!

Slide 22 The answer is NO. We have no information about when edges on the inputs will occur.

Badly-timed input changes could cause setup (or hold) violations – we'll return to this later.

Slide 23 Here we do not have to worry about ill-timed input changes. And we have already done the math ...

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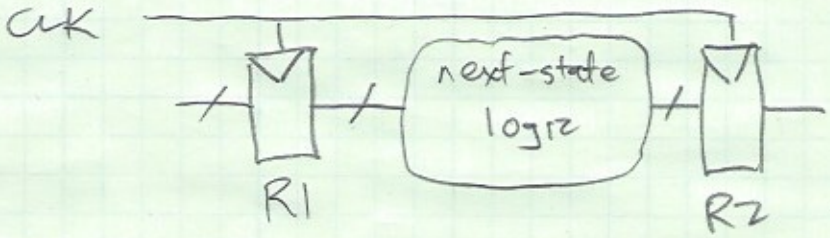

In the FSM R1 and R2 are the same register!
For reliable operation

$$t_{pcq} + t_{pd} \leq T_c - t_{setup}$$

Slides 24-25 A is constant, so we don't need to worry about edges on A. For reliable operation

$$t_{pd} \leq T_c - t_{pcq} - t_{setup}$$

$$T_c = \frac{1}{f_c} = \frac{1}{3.33\,GHz} = \frac{1}{3.33 \times 10^9\,s^{-1}}$$

$$= 0.3 \times 10^{-9}\,s = 300\,ps$$

So for reliable operation,

$$t_{pd} \leq 300ps - 75_{ps} - 35ps = \boxed{190_{ps}}$$

What is t_{pd}. Critical path is NOT → AND4 → OR3.

Overall t_{pd} is $30 + 100 + 110 = \boxed{240\,ps}$

Circuit will not be reliable with a 3.33 GHz clock.

Redesign Implement SOP next-state logic with NAND/NAND instead of AND/OR.

Overall t_{pd} is $\underset{\text{NOT}}{30} + \underset{\text{NAND4}}{80} + \underset{\text{NAND3}}{60} = \boxed{170\,ps}$

Slide 26

$$T_c = \frac{1}{1\,MHz} = \frac{1}{10^6\,s^{-1}} = 10^{-6}\,s = 1000\,ns$$

T_c is very long compared to the timing parameters

Setup time constraints will be easily satisfied.

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