ENEL 353 Section 02 Lecture

Wed Nov 27 2019

Set 9, Slide 45

No matter what the delays are on all the paths from A to the state register, it's always possible that some edge on A will result in an edge on a DFF input within the setup/hold aperture.

Set 9, Slide 46

The synchronizer circuit delays the response of the FSM, but that is often acceptable.

Because edges on A can occur at any time, FF1 will be metastable from time to time. But because it almost never happens that $t_{res} > 0.5T_c$, it is extremely likely that the signal at n1 is a clean 0 or clean 1 by the time t_{setup} starts for FF2. With very high probability, the signal at n2 is ready by t_{p-q} after a rising edge of

CLK, just like the signal coming from the state register.

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