ENEL 353 Section 02 Lecture
Wed Oct 16 2019

Today's lecture may start a few minutes late...

No lecture Fri Oct 18 in Section 02.

5-variable problems (Slides 73-78).

There will be no "doc cam" notes.

Set 6, Slide 5

If S=0, then Y is a copy of D_0

If S=1, then Y is a copy of D_1

Slide 7

(a)

E	state at Y
0	Z (floating/high-impedance)
1	copy of A

(b)

$\overline{E}$	state at Y
0	copy of A
1	Z

(c)

E	state at Y
0	Z
1	copy of $\overline{A}$

(d)

$\overline{E}$	state at Y
0	copy of $\overline{A}$
1	Z

"Active low" signalling is the opposite of the usual convention.

LOW voltage means "on", "go", etc.
HIGH voltage means "off", "stop", etc.

Slide 8

There is no problem with the connection of tristate buffer outputs to each other.
If T0 is enabled, T1 is not enabled and vice versa, so there is never contention.

Slide 9

There are 6 input wires, so a truth table would have 64 rows.
A compact table ...

S_1	S_0	number encoded by S_1S_0	Y
0	0	0	D_0
0	1	1	D_1
1	0	2	D_2
1	1	3	D_3

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Slide 10

(a) two-level SOP logic

Suppose, for example, that $S_1 = S_0 = 0$.

Then $\overline{S}_1\overline{S}_0 = 1$, $\overline{S}_1 S_0 = S_1\overline{S}_0 = S_1 S_0 = 0$

The output of the top AND gate is

$\bar{S}_1 \bar{S}_0 D_0 = 1 \cdot D_0 = D_0$

All the other AND gate outputs are 0.

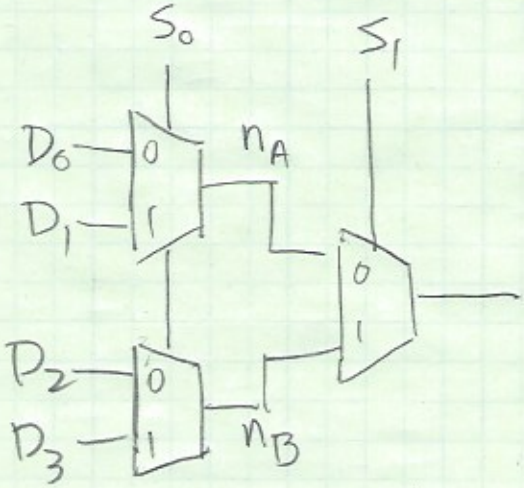
$S_0\ Y = D_0 + 0 + 0 + 0 = D_0$

Similarly, when $(S_1, S_0) = (0, 1)$,

$Y = 0 + D_1 + 0 + 0 = D_1$, and so on.

(b) tristate logic This is similar to the tristate-based 2:1 mux design, but here exactly one of four tristates is enabled at any given time. (Note: Inverters and AND gates are needed to generate $\bar{S}_1\bar{S}_0$, $\bar{S}_1 S_0$, $S_1\bar{S}_0$, $S_1 S_0$.

(c) a "mux tree", built with 3 2:1 muxes



S_1	S_0	n_A	n_B	Y
0	0	D_0	D_2	$n_A = D_0$
0	1	D_1	D_3	$n_A = D_1$
1	0	D_0	D_2	$n_B = D_2$
1	1	D_1	D_3	$n_B = D_3$