ENEL 353 Section 02 Lecture

Mon Oct 21 2019

<u>Midterm</u> - evening of Mon Oct 28

- more details on course home page

<u>Set 6, Slide 12</u>

Select bits for 16:1 mux? 4

Select bits for 32:1 mux? 5

Select bits for N:1 mux? $\log_2 N$ ← general formula

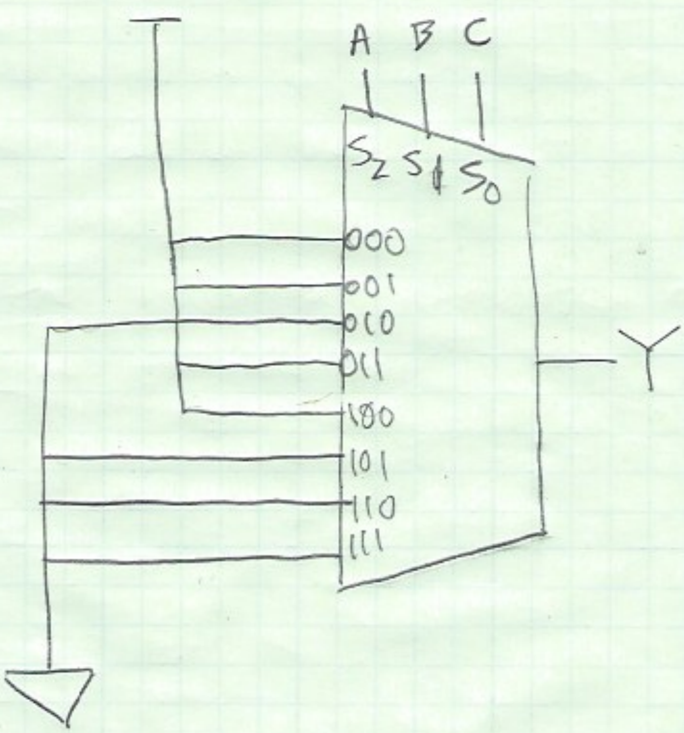
(But the general formula only makes sense if N is a power of two.)

<u>Slide 14</u> Here the output of the AND gate is 0.

<u>Slide 15</u>

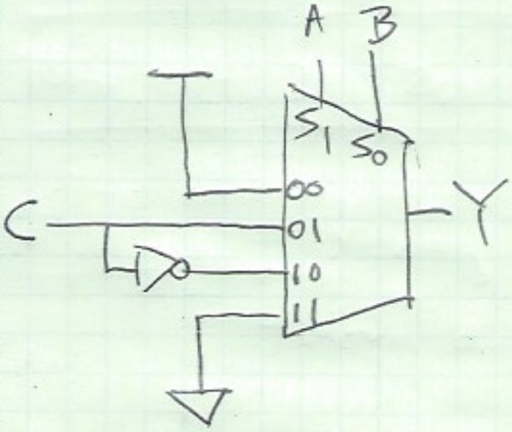
<u>8:1 mux</u>

<u>solution</u>



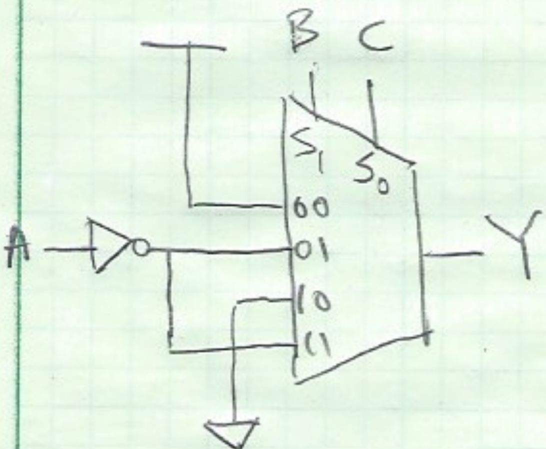
4:1 mux solution

Let's try using (A, B) as (S_1, S_0)



A	B	C	Y	
0	0	0	1	Y = 1
0	0	1	1	
0	1	0	0	Y = C
0	1	1	1	
1	0	0	1	$Y = \overline{C}$
1	0	1	0	
1	1	0	0	Y = 0
1	1	1	0	

4:1 mux solution, using (B, C) as (S_1, S_0)



A	B	C	Y
0	0	0	1
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	0

Y = 1

$Y = \overline{A}$

Y = 0

$Y = \overline{A}$

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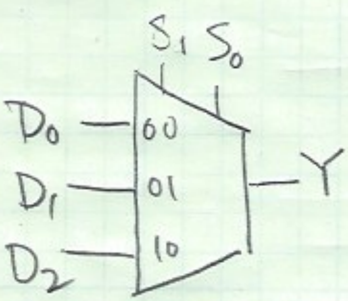
3:1 mux (two different reasonable specifications)



choice 1

S_1	S_0	Y
0	0	D_0
0	1	D_1
1	X	D_2

↑ don't care input

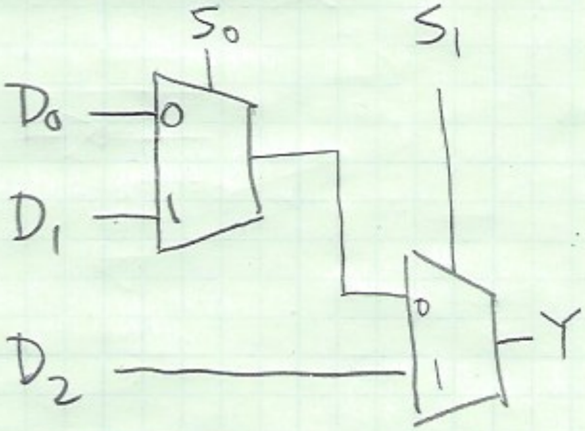
choice 2

S_1	S_0	Y
0	0	D_0
0	1	D_1
1	0	D_2
1	1	X

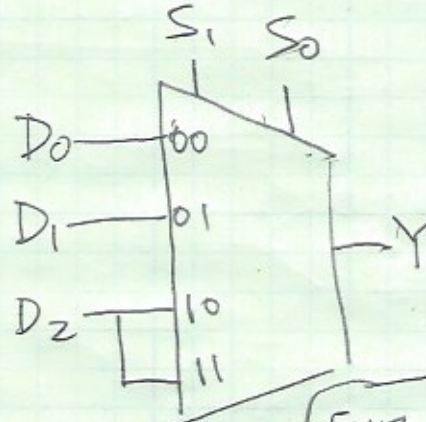
↑ don't care output

Let's go with choice 1

Implementation with two 2:1 muxes



With a 4:1 mux



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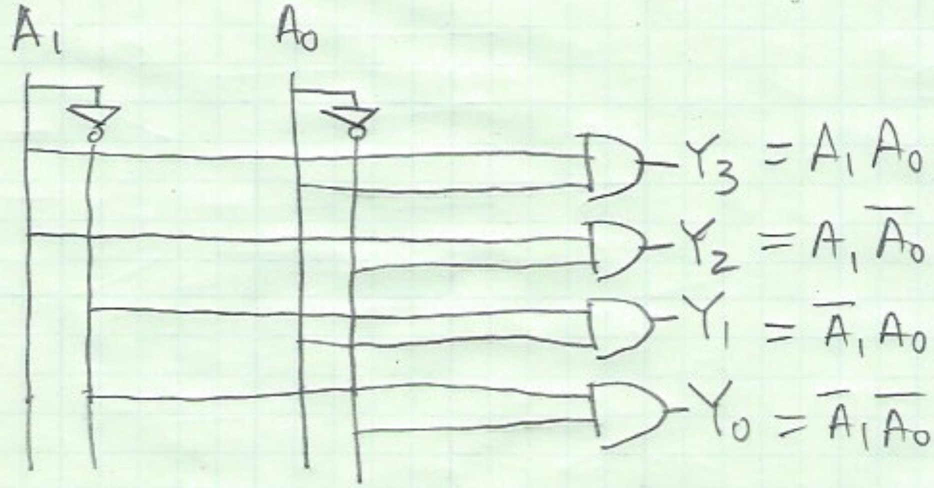
2:4 decoder. Let k be the number encoded by $A_1 A_0$ in unsigned binary. Then $Y_k = 1$ and all the other outputs are 0.

Truth table

A_1	A_0	Y_3	Y_2	Y_1	Y_0
0	0	0	0	0	1
0	1	0	0	1	0
1	0	0	1	0	0
1	1	1	0	0	0

Implementation with NOT and AND gates.



A decoder can be thought of as a "minterm generator."

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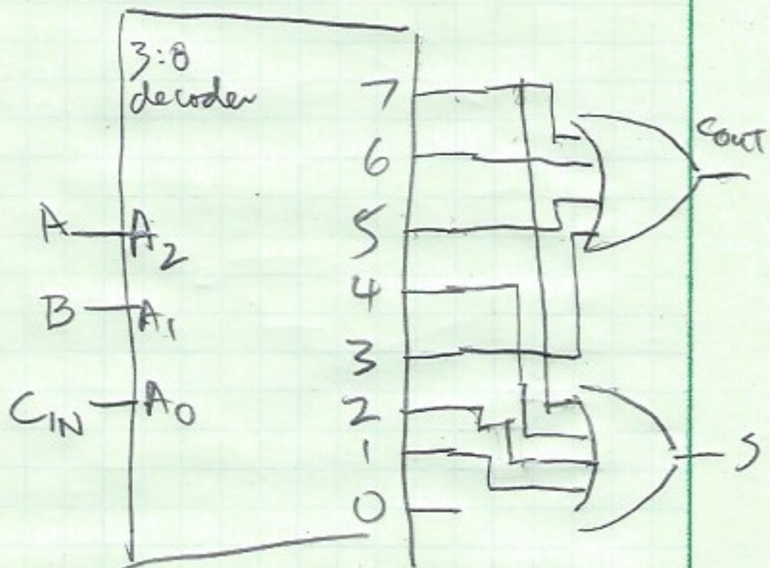
A	B	C_{IN}	C_{OUT}	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1



$C_{OUT} = m_3 + m_5 + m_6 + m_7$

$S = m_1 + m_2 + m_4 + m_7$

Y_0 output of decoder should float. It should NOT be connected to ground – that would cause high current when $(A, B, C_{IN}) = (0, 0, 0)$

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