ENEL 353 Lecture (Section L02)
Fri Oct 25 2019

Room assignment for midterm: Section L02:
KNB 132.

Lab 3 has been posted on D2L.

Set 6, Slide 35

Critical path: This is the slowest possible path from any input to any output. Here it's the path from A or B to Y, through all three gates

$$\text{Overall } t_{pd} = \underset{t_{pd\ AND}}{50} + \underset{t_{pd\ OR}}{60} + \underset{t_{pd\ AND}}{50}$$

$$= 160 \text{ ps}$$

In general, the overall t_{pd} is the sum of t_{pd}'s on the critical path.

Short path - fastest path from any input to any output. For the example, the short is from D to Y through one AND gate. Overall t_{cd} is the sum of t_{cd}'s on the short path. In this example, that is 35 ps.

Slide 36

Critical path From A, B, C or D through the AND4 and OR2 gates.

$$\text{Overall } t_{pd} = 50\text{ps} + 30\text{ps} = \underline{\underline{80\text{ps}}}$$

Short path Same as the critical path in this example!

$$\text{Overall } t_{cd} = 25\text{ps} + 22\text{ps} = \underline{\underline{47\text{ps}}}$$

Remark: The slowest path is not necessarily the one with the most gates.

Slide 37

t_{pd} delay to n1 is $\underbrace{15\text{ps}}_{\text{NOT}} + \underbrace{31\text{ps}}_{\text{AND2}} = 46\text{ps}$

delay to n2 is $\underbrace{40\text{ps}}_{\text{AND3}}$

Therefore the overall t_{pd} is $\underbrace{46\text{ps}}_{\text{longer of delays from inputs to n1, n2}} + \underbrace{42\text{ps}}_{\text{OR}} = 88\text{ps}$

t_{cd} delay to n1 is $\underbrace{25\text{ps}}_{\text{AND2}}$

delay to n2 is $\underbrace{30\text{ps}}_{\text{AND3}}$

So, overall t_{cd} is 25ps + 32ps = 57ps.

25ps: shorter of delays from inputs to n1, n2

32ps: OR2

Slide 39

two-level SOP logic (left side of slide)

let's make a copy of the table from Slide 38

Gate	t_{pd} (ps)
NOT	30
AND2	60
AND3	80
OR4	90
tristate (A to Y)	50
tristate (EN to Y)	35

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t_{pd} from S_1 or S_0 to Out

30 (NOT) + 80 (AND3) + 90 (OR4) = 200ps

t_{pd} from any of $D_0 \ldots D_3$ to Out

80 (AND3) + 90 (OR4) = 170ps

tristate logic (right side of slide)

t_{pd} from S_1 or S_0 to Out

30 (NOT) + 60 (AND2) + 35 (tristate EN to Y) = 125ps

t_{pd} from any of $D_0 \ldots D_3$ to Out

50ps - tristate A to Y

Slide 40 Clearly Y reacts more slowly to a change in S_0 than to a change in S_1.

t_{pd} from S inputs to Y

$= \underset{\text{tristate En to Y}}{35} + \underset{\text{tristate A to Y}}{50} = 85\text{ ps}$

t_{pd} from D inputs to Y

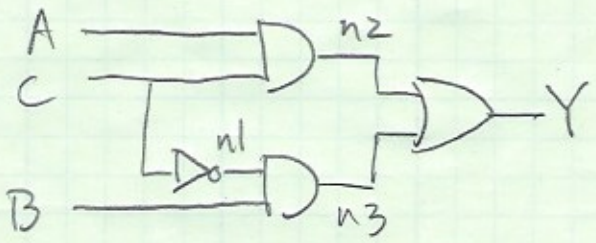
$= \underset{\text{tristate A to Y}}{50} + \underset{\text{tristate A to Y}}{50} = 100\text{ ps}$

Slide 42

When (A, B, C) = (1, 1, 1), Y = 1
When (A, B, C) = (1, 1, 0), Y = 1
Ideally, then, when (A, B, C) switches from (1, 1, 1) to (1, 1, 0), Y stays at 1.

Timing diagram: See Slide 43.

The circuit:



The brief drop in Y between t = 110ps and t = 140ps is an example of what is called a glitch, caused by delays in logic gates.