ENEL 353 Section 02 Lecture
Mon Oct 28 2019



Midterm - tonight! See course home page for details.

Lab 3 - this week and next week

Quiz 3 - Tue Nov 5
Set 7, Slide 7

$R=1, S=0$

$Q=0$ because $R=1$

$QN = \overline{(S+Q)} = \overline{(0+0)} = 1 \quad (Q, QN) = (0,1)$

$R=0, S=1$

$QN=0$ because $S=1$

$Q = \overline{(R+QN)} = \overline{(0+0)} = 1 \quad (Q, QN) = (1,0)$

$R=1, S=1$

$Q=0$ because $R=1$

$QN=0$ because $S=1$

$(Q, QN) = (0,0)$

This is why your instructor does not like to call the second output $\overline{Q}$.

$R=0, S=0$ (The interesting case!)

$Q = \overline{(R+QN)} = \overline{(0+QN)} = \overline{QN}$

$QN = \overline{(S+Q)} = \overline{(0+Q)} = \overline{Q}$

Two solutions!

$(Q, QN) = (0,1)$

$(Q, QN) = (1,0)$

Slide 8

## Useful behaviour of an SR latch

Prior to the time window shown in the slide, (Q, QN) somehow got to (0, 1).

The first pulse on S forces (Q, QN) to (1, 0).

The 2nd pulse on S leaves (Q, QN) at (1, 0)

The first pulse on R forces (Q, QN) to (0, 1)

The 2nd pulse on R leaves (Q, QN) at (0, 1).

S stands for set – turn Q ON

R stands for reset – turn Q OFF

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## Problematic behaviour, Part 1

When S=R=1, QN does not perform its normal of providing $\overline{Q}$.

## Problematic behaviour, Part 2

What if S and R both make 1 → 0 transitions at nearly the same time?

- (Q, QN) could go quickly to (0, 1)
- " " " " " (1, 0)
- Both outputs could "stick" for a while between logic 0 and logic 1, then eventually the state would go to (0,1) or (1,0). This phenomenon is called metastability
- Exact behaviour is not predictable!

Slide 12

$f_c = 2.5\ GHz \quad T_c = \frac{1}{2.5\ GHz} = \frac{1}{2.5 \times 10^9\ s^{-1}}$

$= \frac{1}{2.5} \times 10^{-9}\ s = 0.4\ ns = 400\ ps$

Slide 17

When CLK = 0 R = S = 0

When CLK = 1 $R = \overline{D}$, $S = D$ } Only one of R and S is 1

The problematic case of R = S = 1 can't happen, so QN will always be equal to $\overline{Q}$.

Slide 18 – To emphasize the basic behaviour, we won't show delays in the timing diagram for this circuit.

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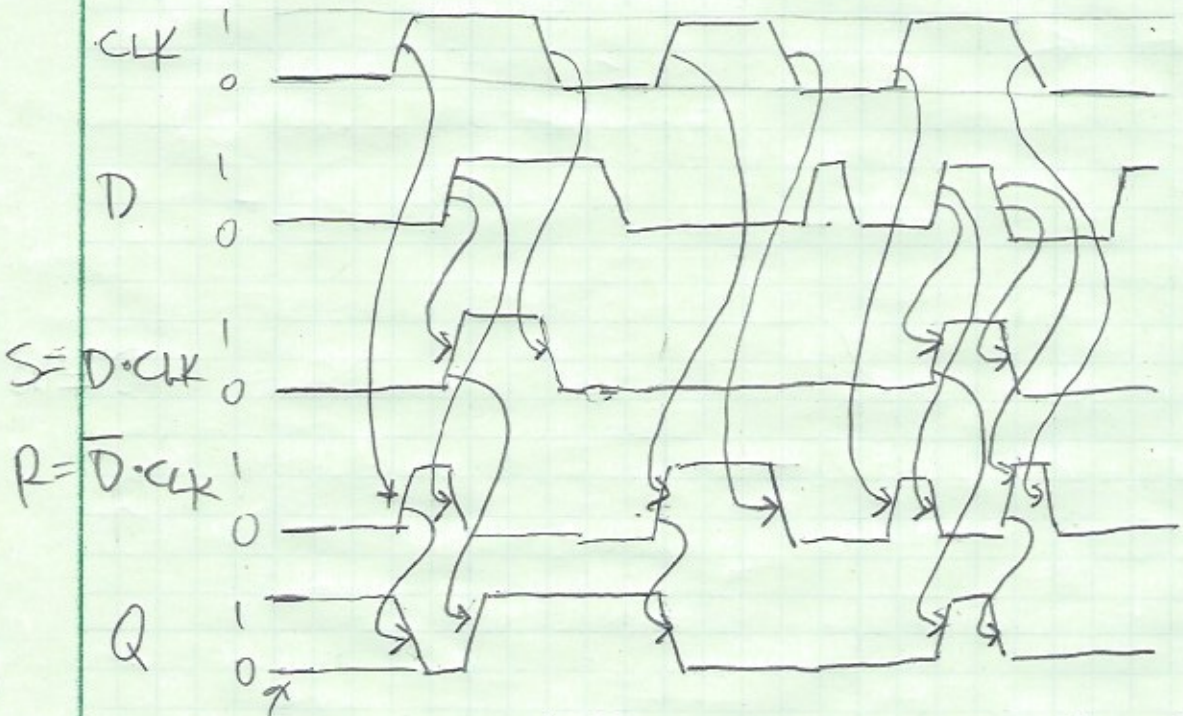


Here we show both possible initial states for Q (unlike what's on the slide).

When CLK is HIGH, the latch is said to be transparent. Changes to D are (almost) immediately visible on Q. In other words, when CLK is HIGH, Q follows D.

When CLK is LOW, the latch is said to be opaque. Q holds on to whatever value Q had when CLK most recently went 1 → 0.

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