ENEL 353 Section 02 Lecture

Wed Oct 30 2019

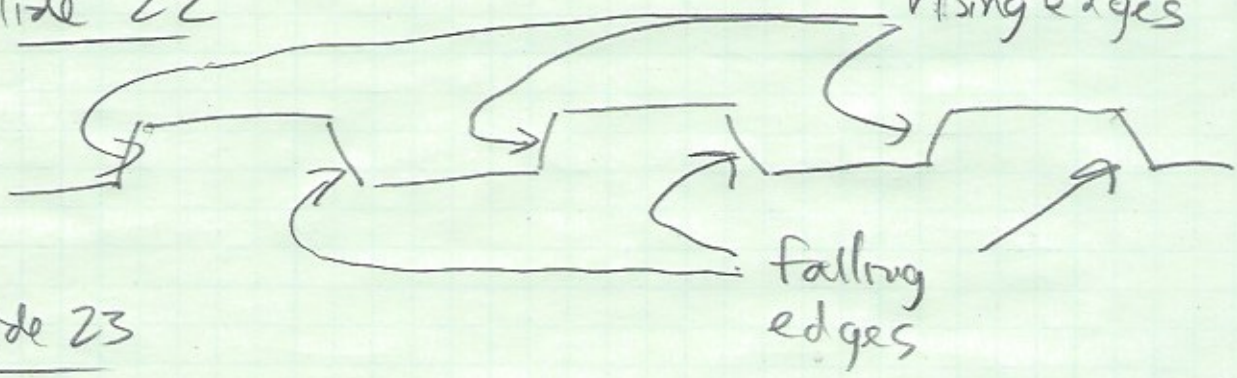
Quiz #3 - Tue Nov 5

Set 7, Slide 18

A D latch is said to be level-sensitive with respect to CLK - Q follows D or ignores D based on the level (LOW or HIGH) of CLK.

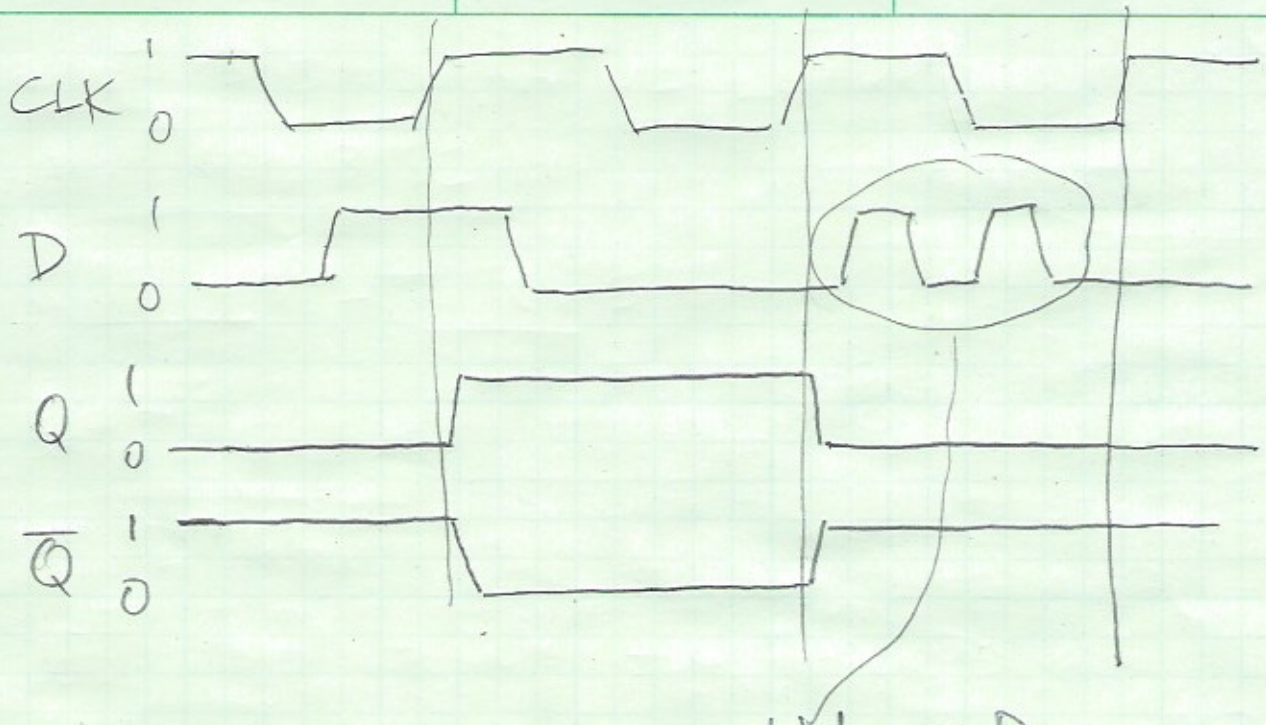
(We'll see soon that a D flip-flop is not level-sensitive - instead it's edge-triggered with respect to CLK.)

Slide 22



Slide 23

D flip-flop behaviour



glitches on D
between rising edges of CLK
have no effect on $(Q, \overline{Q})$

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Master latch – goes opaque when the flip-flop CLK goes HIGH – that is, on a rising edge of that CLK. So the signal at N1 will be the value "grabbed" when the FF CLK had a rising edge, and N1 persists in that state for half a clock cycle.

Slave latch – is transparent for the first half of a cycle. So Q_{OUT} = N1 during that time. For the second half of the cycle, the latch is opaque and holds the value N1 had when the FF CLK went LOW.

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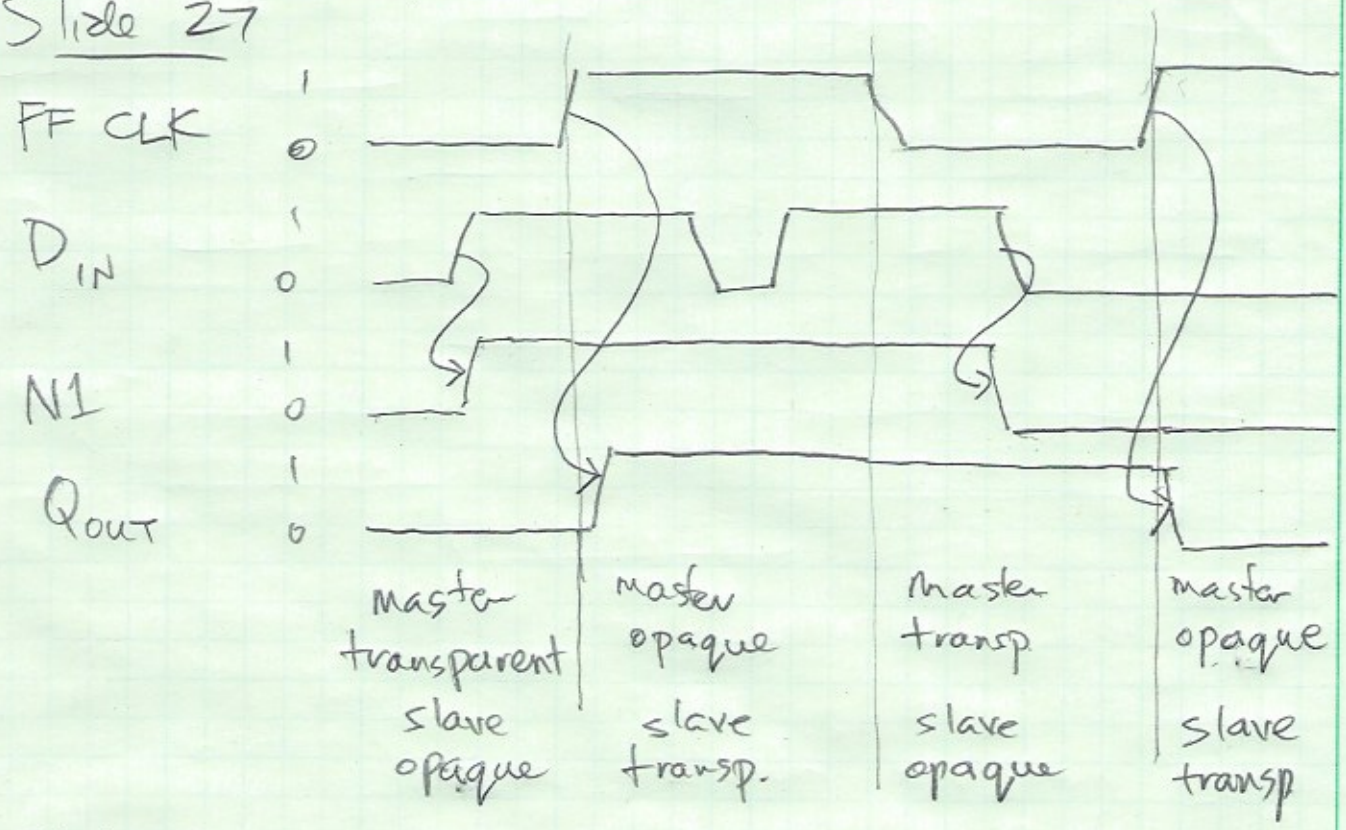
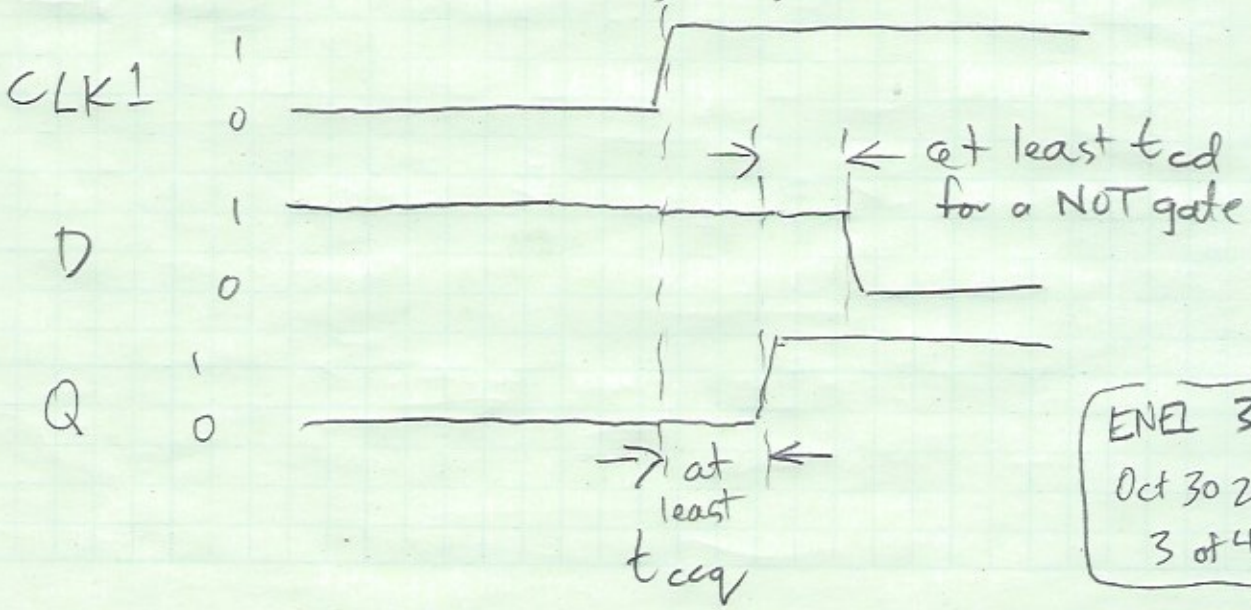


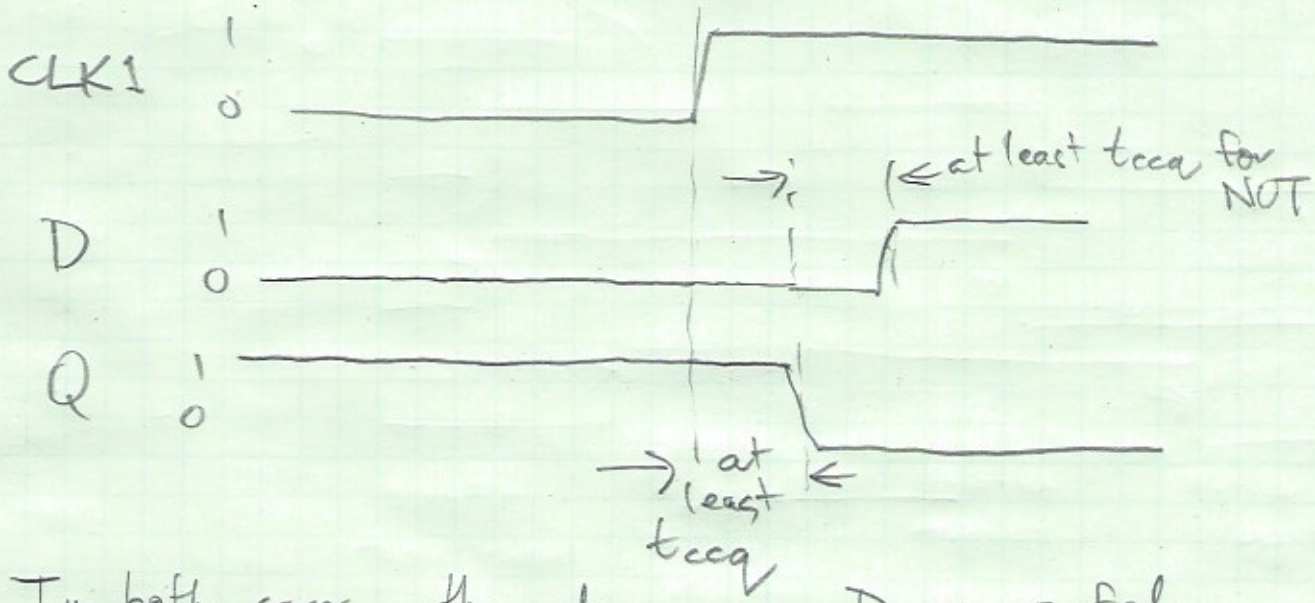
Slide 30

t_{ccq} is clock-to-Q contamination delay, the shortest possible delay between a rising on the CLK input of a DFF and a change in the Q output of that DFF.

Q=0 just before a rising edge of CLK1



Q=1 just before a rising edge of CLK1



In both cases, the change in D is safely separated by at least $t_{ccq} + t_{cd\_NOT}$ from the rising CLK edge, so changes in Q will be predictable.

Slide 32 If $f_{CL1} = 100 \times 10^3$ Hz, then

$$T_{CLK1} = \frac{1}{10^5 s^{-1}} = 10^{-5} s = 10,000,000 ps$$

The period of CLK1 is so long that the edges of CLK1 and CLK2 appear to be perfectly vertical and aligned.

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