ENEL 353 Section 02 Lecture
Fri Sept 20 2019

Set 2, Slide 31

(a) +0.9V is in the forbidden zone.
We can't say what the output will be.

(b) +0.7V < V_{IL}, read as logic 0
+2.1V > V_{IH}, read as logic 1
XOR output is logic 1, so must be between +2.4V and +5.0V

(c) +2.2V > V_{IH}, read as logic 1
+0.6V < V_{IL}, read as logic 0
NOR output is logic 0, so between 0V and 0.4V.

(d) Two inputs will be read as logic 1.
But +1.9V is in the forbidden.
Output is unknown.

Slides 32-34

Slide 33 All three plots are okay.
When $V_{IN} \leq V_{IL}$, $V_{OUT} \geq V_{OH}$.
And when $V_{IN} \geq V_{IH}$, $V_{OUT} \leq V_{OL}$.

Slide 34

Purple curve – bad because $V_{OUT} > V_{OL}$ for some $V_{IN} \geq V_{IH}$.

Orange curve – bad because $V_{OUT} < V_{OH}$ for some $V_{IN} \leq V_{IL}$.

Slide 37

Noise margins for low-level CMOS

$$NM_L = V_{IL} - V_{OL} = 0.9V - 0.36V = 0.54V$$

$$NM_H = V_{OH} - V_{IH} = 2.7V - 1.8V = 0.9V$$

If NOT gate 1 input is +3.1 V

That's a logic 1. Output of NOT gate 1 will be $\leq V_{OL} = 0.36V$. NOT gate 2 will reliably read a 0 input as long as the added noise is less than 0.54V.

If NOT gate 1 input is +0.2V

That is a logic 0. Output of NOT gate 1 will be $\geq V_{OH} = 2.7V$. NOT gate 2 will reliably read a 1 input as long as the added is greater than −0.9V. (In other words, noise magnitude must be less than NM_H.

Slide 42

Generic symbols for combinational logic

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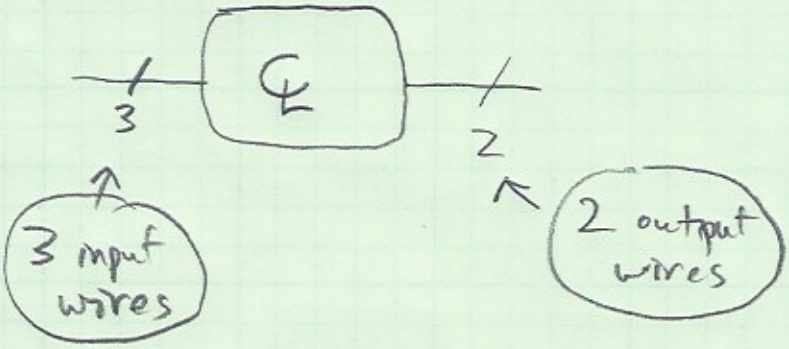
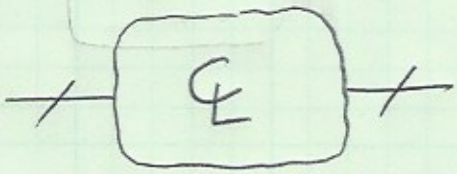
3-input, 2-output

3-input, 2-output, another notation ("bus" notation)



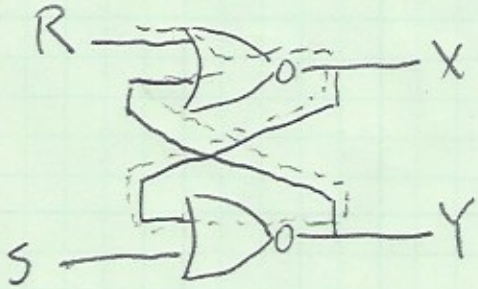
unspecified numbers of inputs and outputs



here slash says "more than one wire"

Slide 44

(a)



Does not satisfy rule about cyclic paths.

(b) Output node Y connects to outputs of two elements - not allowed.

(c) satisfies all three rules.

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Slide 45

(a) satisfies all 3 rules

(b) has a cyclic path