T02 Tutorial Slides for Week 13

ENEL 353: Digital Circuits — Fall 2019 Term

Steve Norman, PhD, PEng

Electrical & Computer Engineering
Schulich School of Engineering
University of Calgary

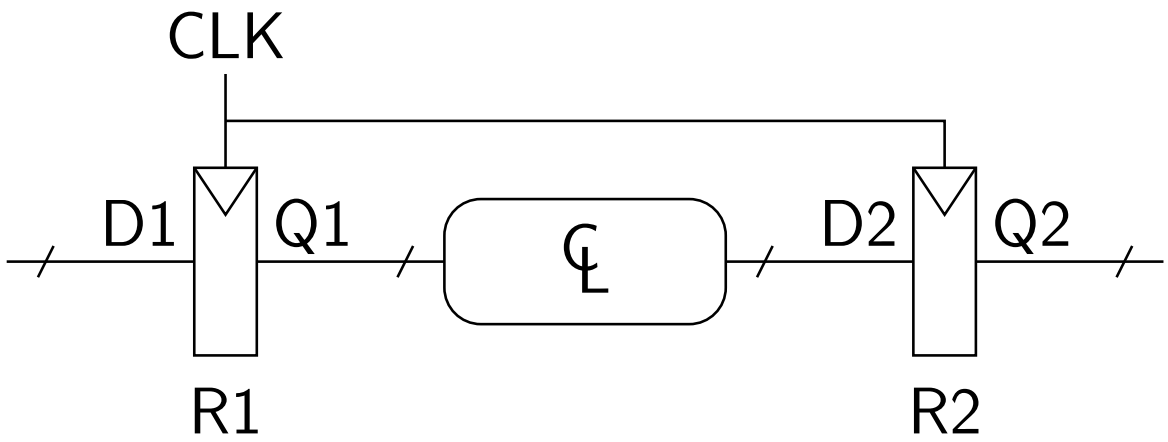
3 December, 2019

Topics for today

Timing of sequential logic.

A ROM-based FSM design.

Exercise 1: Derivation of timing constraints

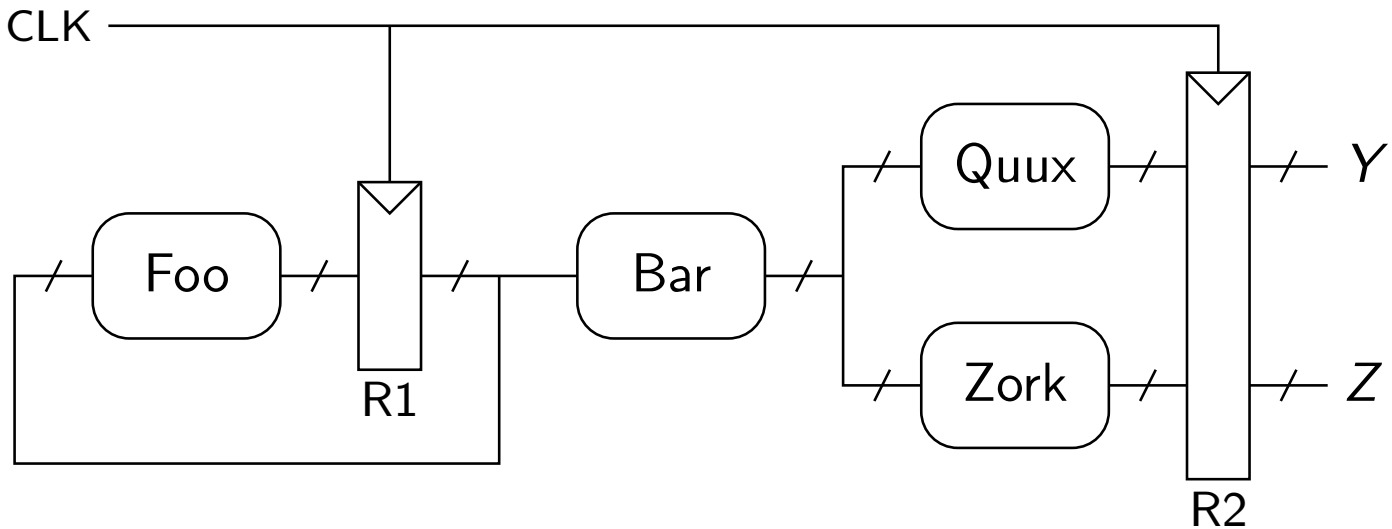


The math for this is very easy. The hard part is remembering what the problem specifications are! If you practice the derivations a few times, it may help you remember.

Let's assume that the input to R1 is well-behaved, that R1 and R2 have the same values for timing parameters, and that there is no clock skew.

Let's derive inequalities that, when true, guarantee that setup-and-hold-time violations cannot happen at the input to R2.

Exercise 2: Application of timing constraints

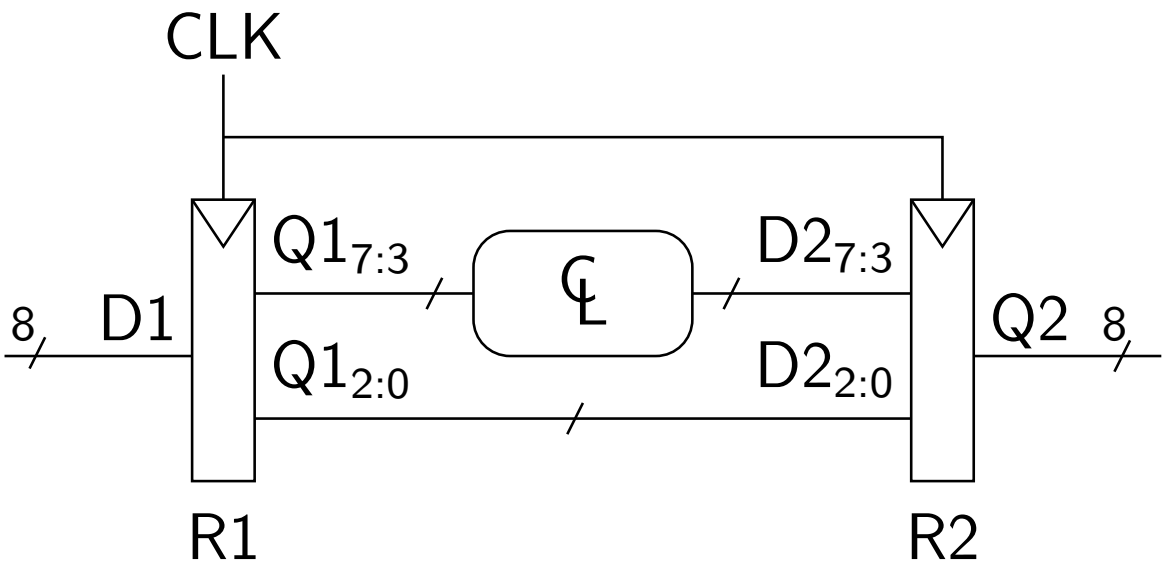


Foo, Bar, Quux, and Zork are all combinational logic with these values for t_{pd}, in ps: 250 for Foo, 60 for Bar, 100 for Quux, and 180 for Zork.

For both R1 and R2, $t_{\text{setup}} = 75\,\text{ps}$ and $t_{\text{pcq}} = 33\,\text{ps}$.

What is the minimum clock period for reliable operation of the circuit? (Assume that there is no clock skew.)

Exercise 3: Timing constraints, no clock skew

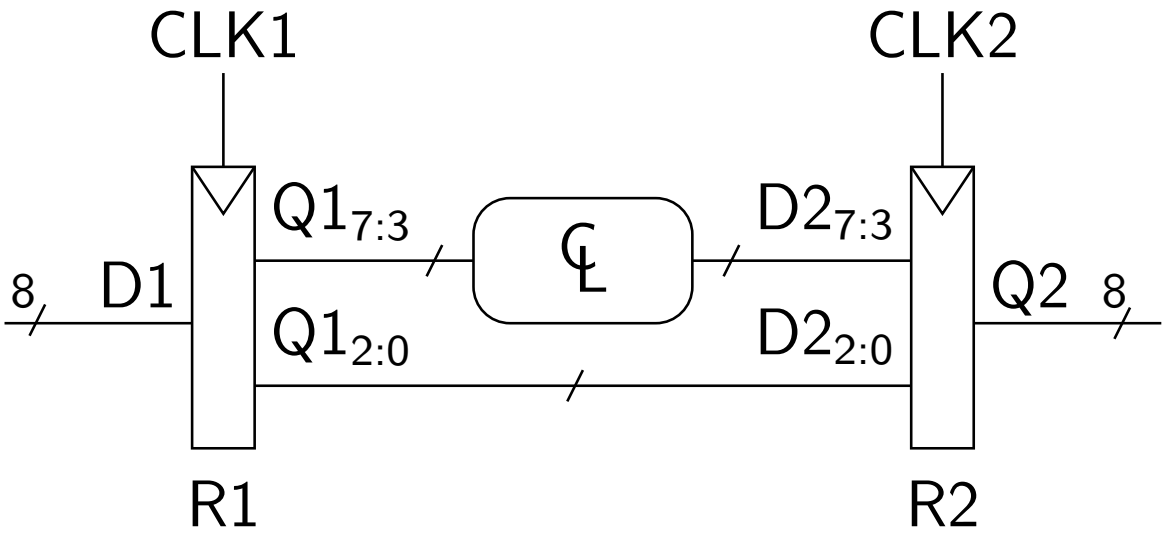


For registers,
$t_{\text{setup}} = 25\,\text{ps}$,
$t_{\text{hold}} = 10\,\text{ps}$,
$t_{\text{pcq}} = 50\,\text{ps}$,
$t_{\text{ccq}} = 30\,\text{ps}$.

Is there any possibility of a hold time violation at R2?

If the desired T_C is 500 ps, what constraints are there on the timing parameters of ℄?

Exercise 4: Timing constraints with clock skew



For registers,
$t_{\text{setup}} = 25\,\text{ps}$,
$t_{\text{hold}} = 10\,\text{ps}$,
$t_{\text{pcq}} = 50\,\text{ps}$,
$t_{\text{ccq}} = 30\,\text{ps}$.

For ⏚,
$t_{\text{pd}} = 350\,\text{ps}$,
$t_{\text{cd}} = 200\,\text{ps}$.

CLK1 and CLK2 come from the same source, with $T_C = 500\,\text{ps}$, but there may be some clock skew.

What is the maximum t_{skew} for reliable behaviour of R2?

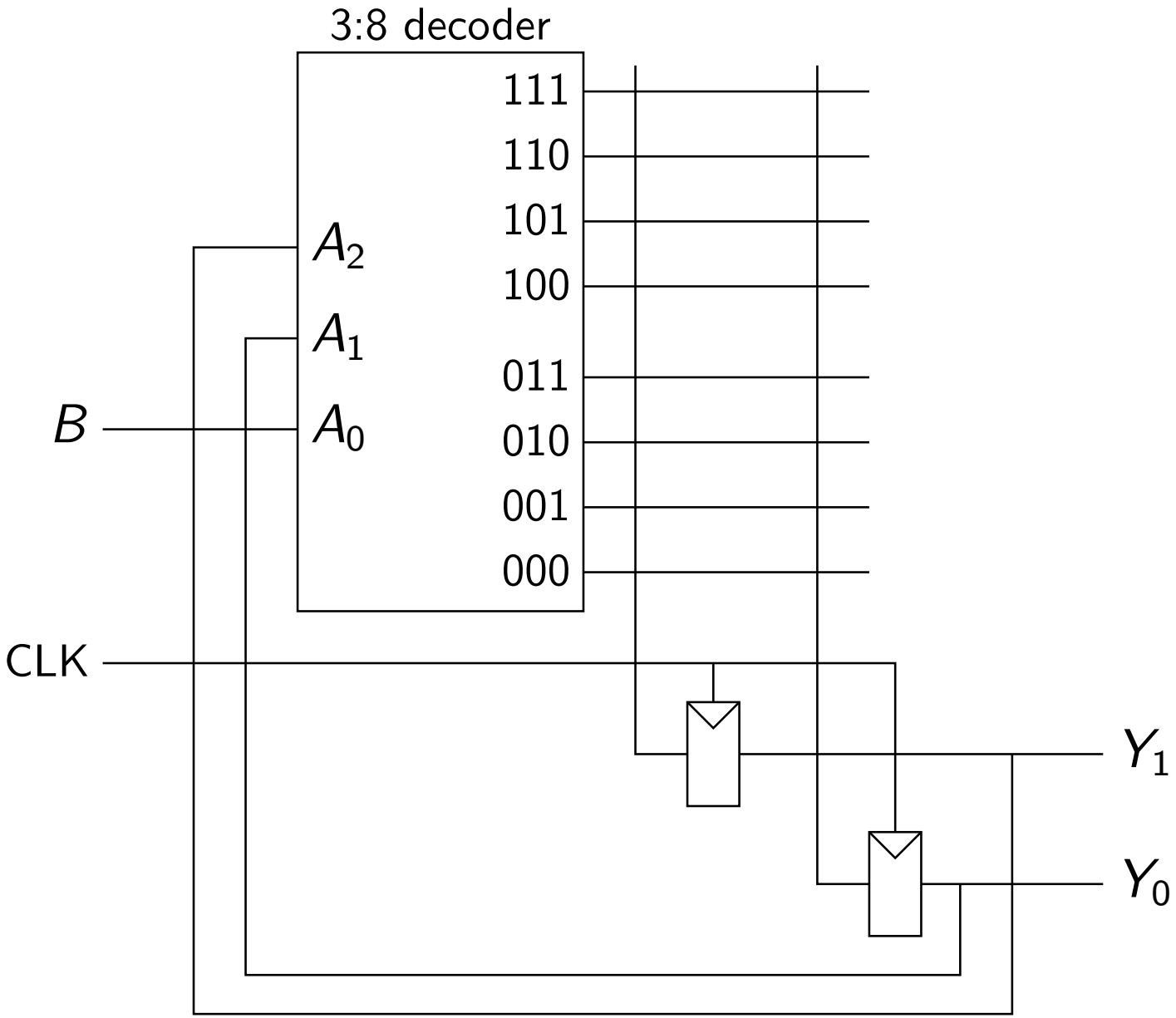
Suppose that buffers are available with $t_{\text{pd}} = 45\,\text{ps}$ and $t_{\text{cd}} = 35\,\text{ps}$. How can they be used to allow the circuit to tolerate $t_{\text{skew}} = 70\,\text{ps}$?

Exercise 5: A ROM-based FSM

Let's copy the schematic on the next slide, then solve following problem ...

Put dots on the ROM array to complete the design of a counter with 1-bit input B and a two-bit output $Y_{1:0}$, such that

- when $B = 1$ the output should go through the cycle 00, 01, 10, 11, 00, 01, and so on, changing on each rising edge of CLK;
- when $B = 0$ the output should stay frozen from one clock cycle to the next.


3:8 decoder
111
110
101
100
011
010
001
000
A_2
A_1
A_0
B
CLK
Y_1
Y_0