T02 Tutorial Slides for Week 9

ENEL 353: Digital Circuits — Fall 2018 Term

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30 October, 2018

Topics for today

Multiplexers and decoders.

Practice with sequential devices: SR latches, D latches and D flip-flops.

Timing considerations for adder designs.

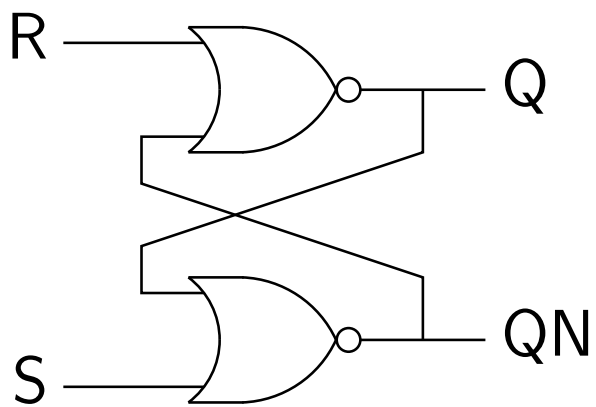
Exercise 1: Multiplexers and decoders

Part a: Make a circuit for the truth table using an inverter and two 4:1 multiplexers.

Part b: Make a circuit for the truth table using a 3:8 decoder and two OR gates.

A	B	C	F	G
0	0	0	0	1
0	0	1	1	0
0	1	0	1	0
0	1	1	0	0
1	0	0	1	0
1	0	1	1	0
1	1	0	0	1
1	1	1	0	1

Review: NOR-based SR latch



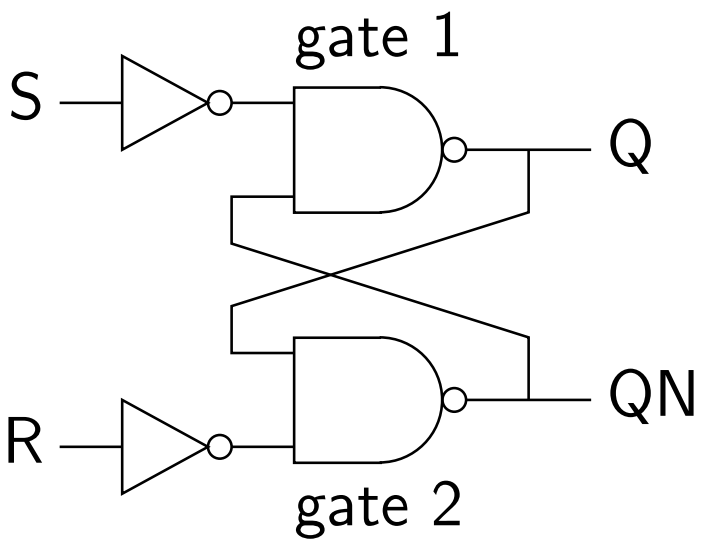
We've seen in a lecture that the outputs will be:

R	S	Q	QN
0	0	see below	
0	1	1	0
1	0	0	1
1	1	0	0

When $R = S = 0$, (Q, QN) will be $(0, 1)$ if the most recent pulse was on R, and $(1, 0)$ if the most recent pulse was on S.

If pulses on R and S end at nearly the same time, behaviour is unpredictable.

Exercise 2: NAND-based SR latch



Let's do some algebra to complete the following table:

R	S	Q	QN
0	0		
0	1		
1	0		
1	1		

Remark:

The course textbook suggests on page 112 that for an SR latch, when $R = S = 1$, (Q, QN) must be $(0, 0)$.

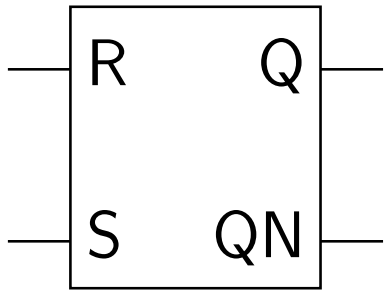
But for the NAND-based SR latch on the previous slide, that isn't true.

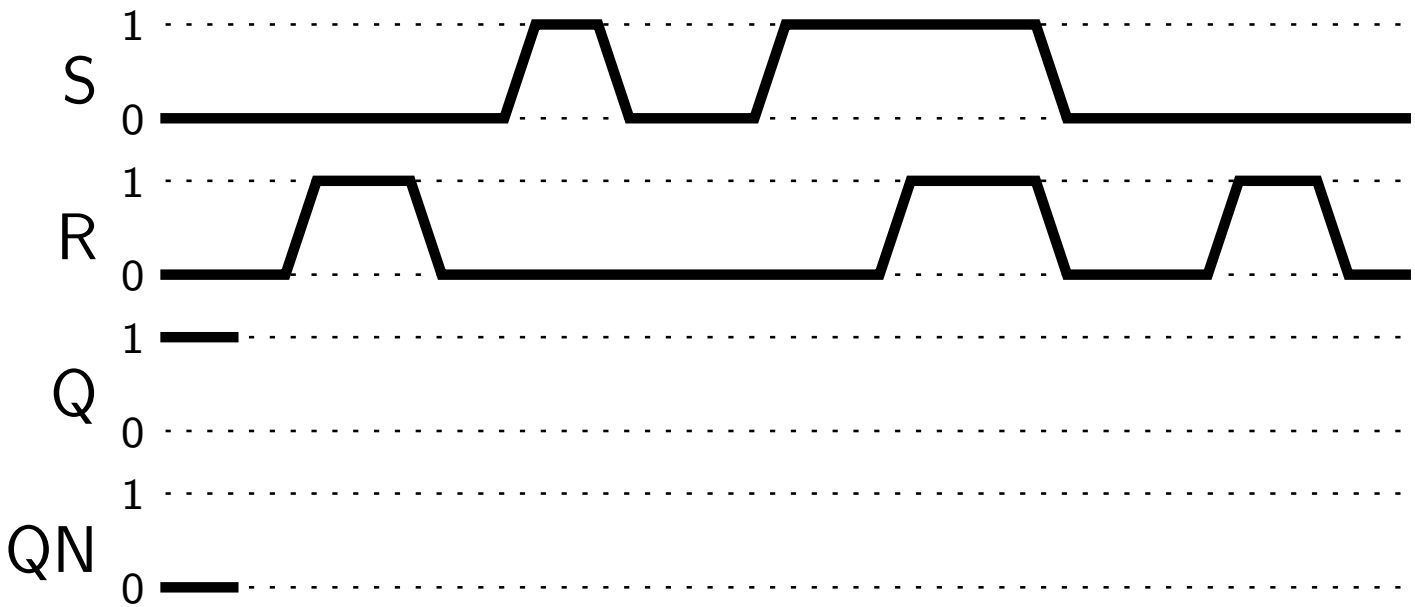
It's not worthwhile to worry much about this issue, because for normal operation of an SR latch, situations where $R = S = 1$ should be **avoided**.

Exercise 3: More about SR latches

Complete the timing diagram to the best of your ability.

Why is it that during a certain interval, it's not possible to be precise about the values of Q and QN?

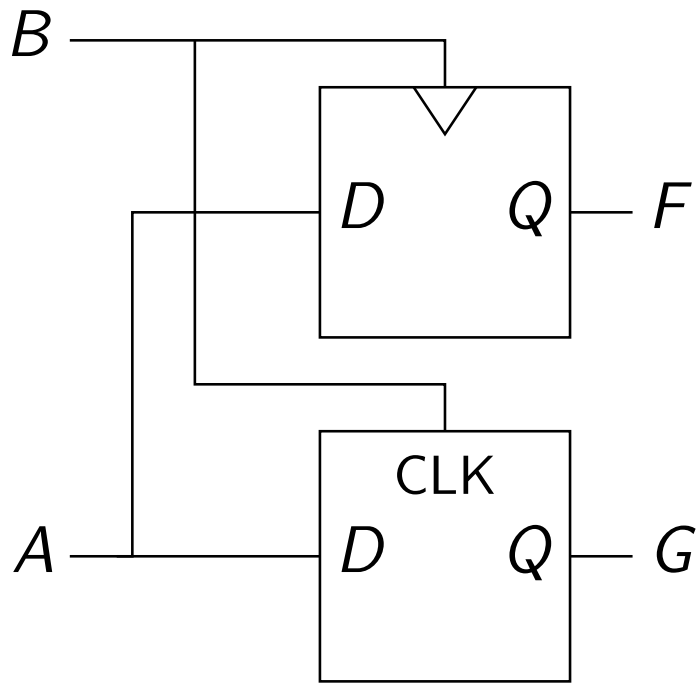


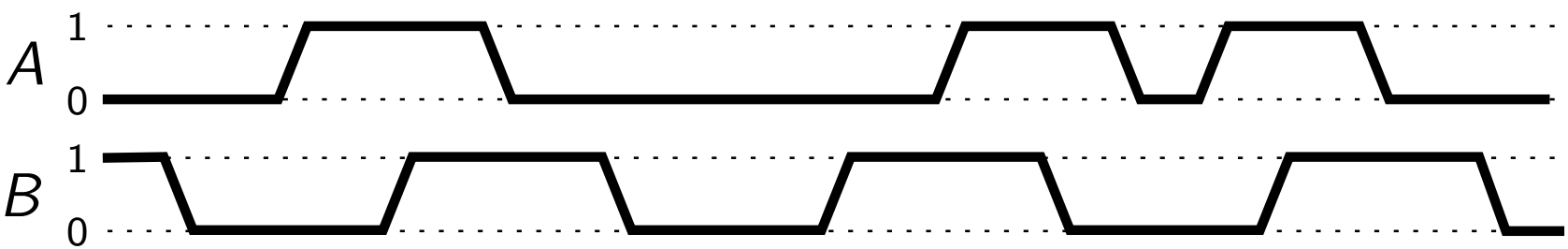


Exercise 4: D latch versus D flip-flop

(i) Write one-or-two-sentence descriptions of the behaviours of D latches and D flip-flops.

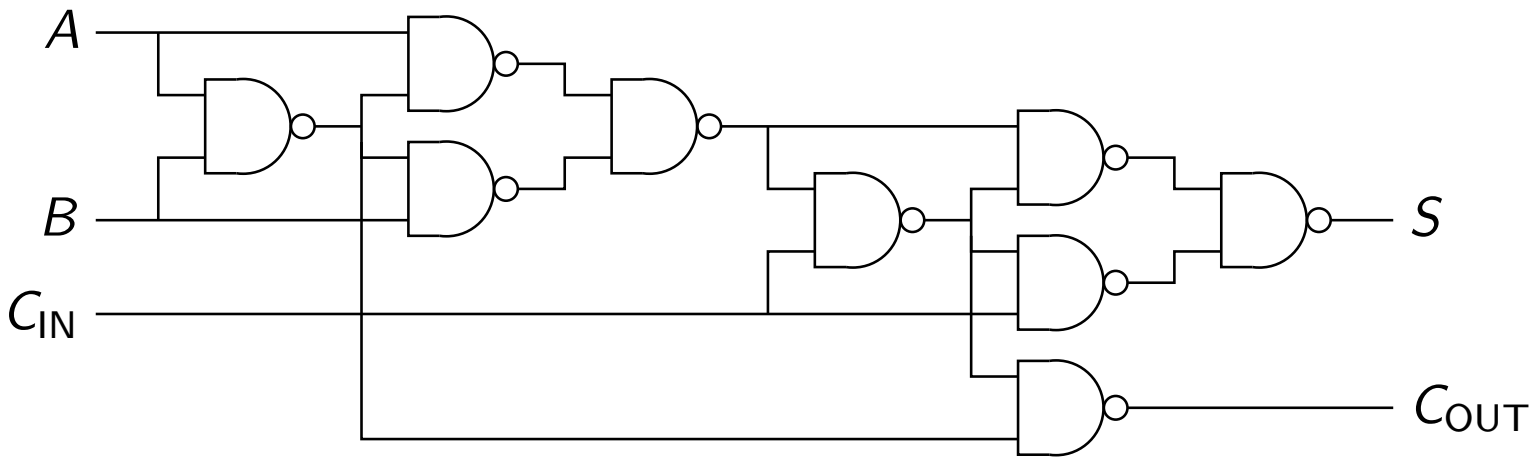
(ii) If A and B are functions of time, as given below, what are F and G as functions of time?





Exercise 5: Timing for a NAND-based full adder

Here is an implementation of a 1-bit full adder using 9 NAND2 gates. (It's true but **not obvious** that it implements the adder functions correctly!)

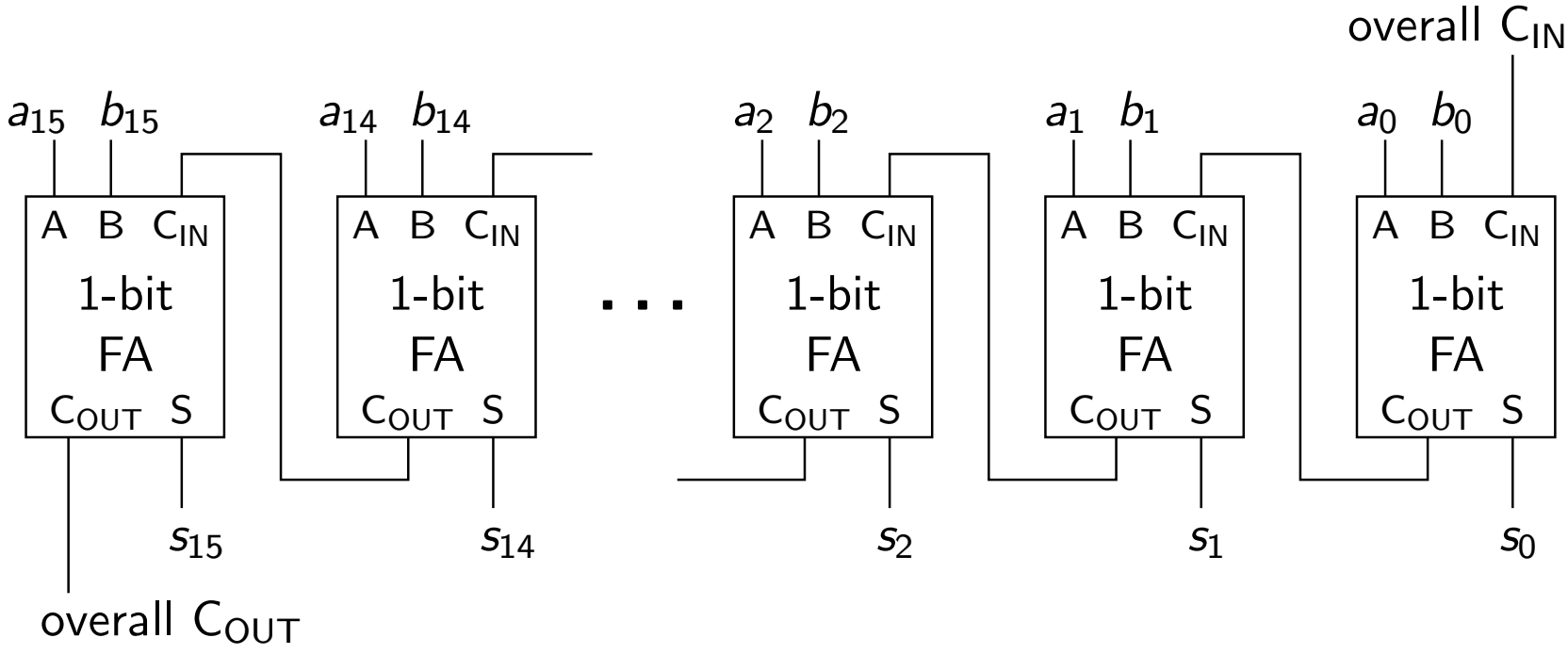


Suppose that for a NAND2 gate, $t_{cd} = 29\,\text{ps}$ and $t_{pd} = 40\,\text{ps}$.

What is the overall t_{cd} for the circuit?

What is t_{pd} from A or B to S? From A or B to C_{OUT}? From to C_{IN} to S? From to C_{IN} to C_{OUT}?

Exercise 6: Adder timing



Assuming the 1-bit full adder design of Exercise 5, determine the overall t_{pd} for the above circuit.

Comment on why the smallest t_{pd} in the circuit of Exercise 5 was designed to be the delay from C_{IN} *to* C_{OUT}.