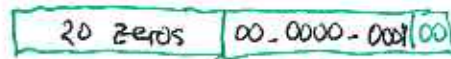


Address : 0x0000_0004



tag = 0 set = 1

0x0000_000c

tag = 0 set = 3

0x0000_0008

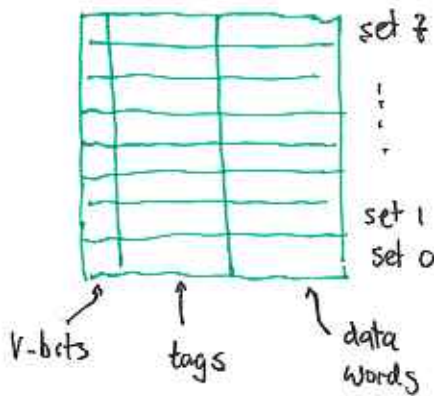
tag = 0 set = 2

On 5 times through this loop, there will be

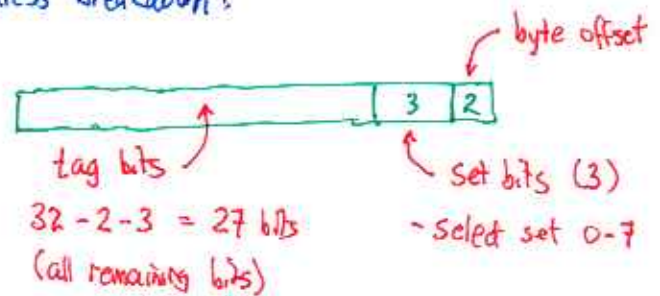
- 3 misses (first time through loop)
- 12 hits (next four loops)

Hit rate = 80% , miss = 20%

Example : Direct-mapped caches with 8 sets

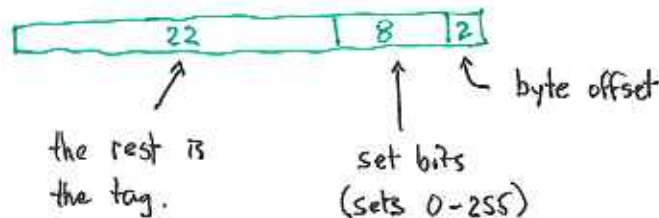


Address breakdown :



Set-bit conflicts - problems with direct-mapped caches

Say, for example, we have a direct-mapped cache with 256 sets.



And suppose we have two C functions

foo() → at address 0x0040_3540

bar() → at address 0x0041_3540

$foo \rightarrow 0x00403540$ $\left| \begin{array}{l} 0000-0000-0100-0000-0011-01 \\ \text{tag} = 0x00100d \end{array} \right| \begin{array}{l} 01-0100-00 \\ \text{set} = 80_{10} \end{array} \left| 00 \right.$
 $bar \rightarrow 0x00413540$ $\text{tag} = 0x00104d$ $\text{set} = 80_{10}$

```

C-code:   for (i=0; i<n; i++) {
           x = foo();
           bar(x);
           }

```

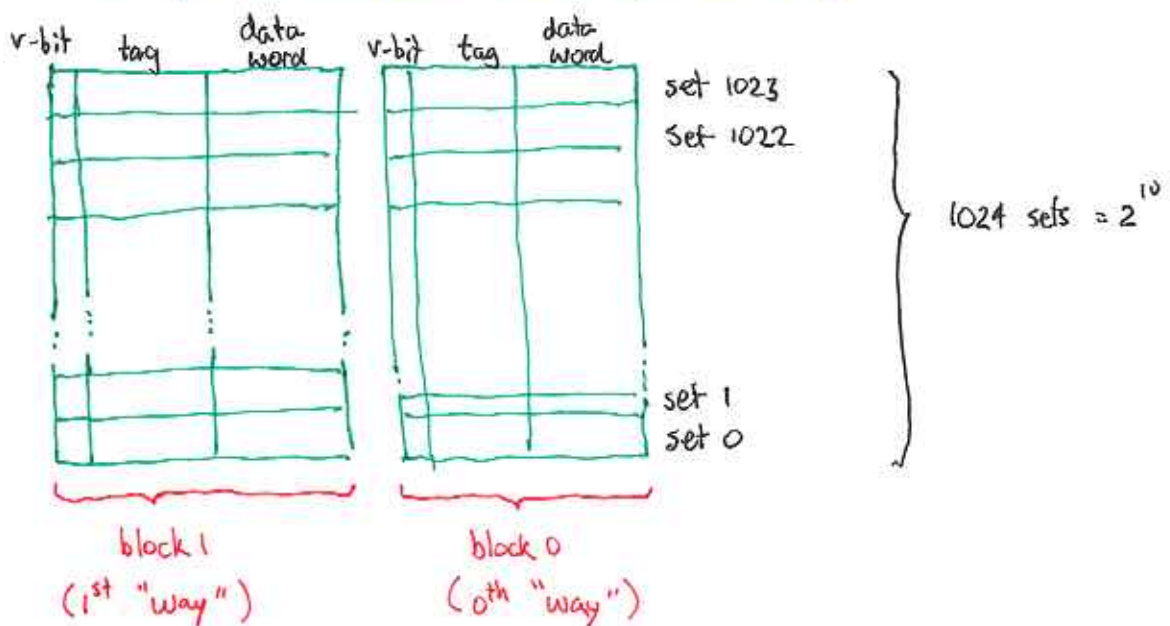
Both procedures have the same 8-bit set no. (80)

- calls to $foo()$ and $bar()$ cause caches misses every time
- this is a cache conflict called a set-bit conflict.
- happens in I-caches as well as D-caches.

Solution — set-associative caches

Definition: An N-way set-associative cache is where a word with a given address can be in any one of N places in a single set of the cache.

Layout of a 2-way set-associative cache (10 set bits)



Address breakdown is the same as our previous example; e.g.,
0x0040_3540

$$\underbrace{0000-0000-0100-0000-0011}_{20\text{-bit tag}} \quad \underbrace{0101-0100-00}_{10\text{ set bits (0x150)}} \quad \underbrace{00}_{\text{byte offset}}$$

Set-associative caches allow addresses with the same set bits but different tags to coexist in the same set.

- E.g., for a cache lookup on set 0x150, both entries are checked simultaneously for a hit.
- A hit is when exactly one entry found with $v=1$ and matching tag.

Multiple matches cannot occur.

- hardware prevents same memory word from being cached in more than one place.

- Notes:
- foo () and bar () can be in the cache at the same time.
 - fewer misses than a direct-mapped cache
 - some set-associative caches can be multi-word.
(some Intel processors have 8-way set-associative, 64 bytes per block, 8 64-bit words)

Fully associative caches

A special cache in which there is:

- just one set (a really wide one)
- contains N ways