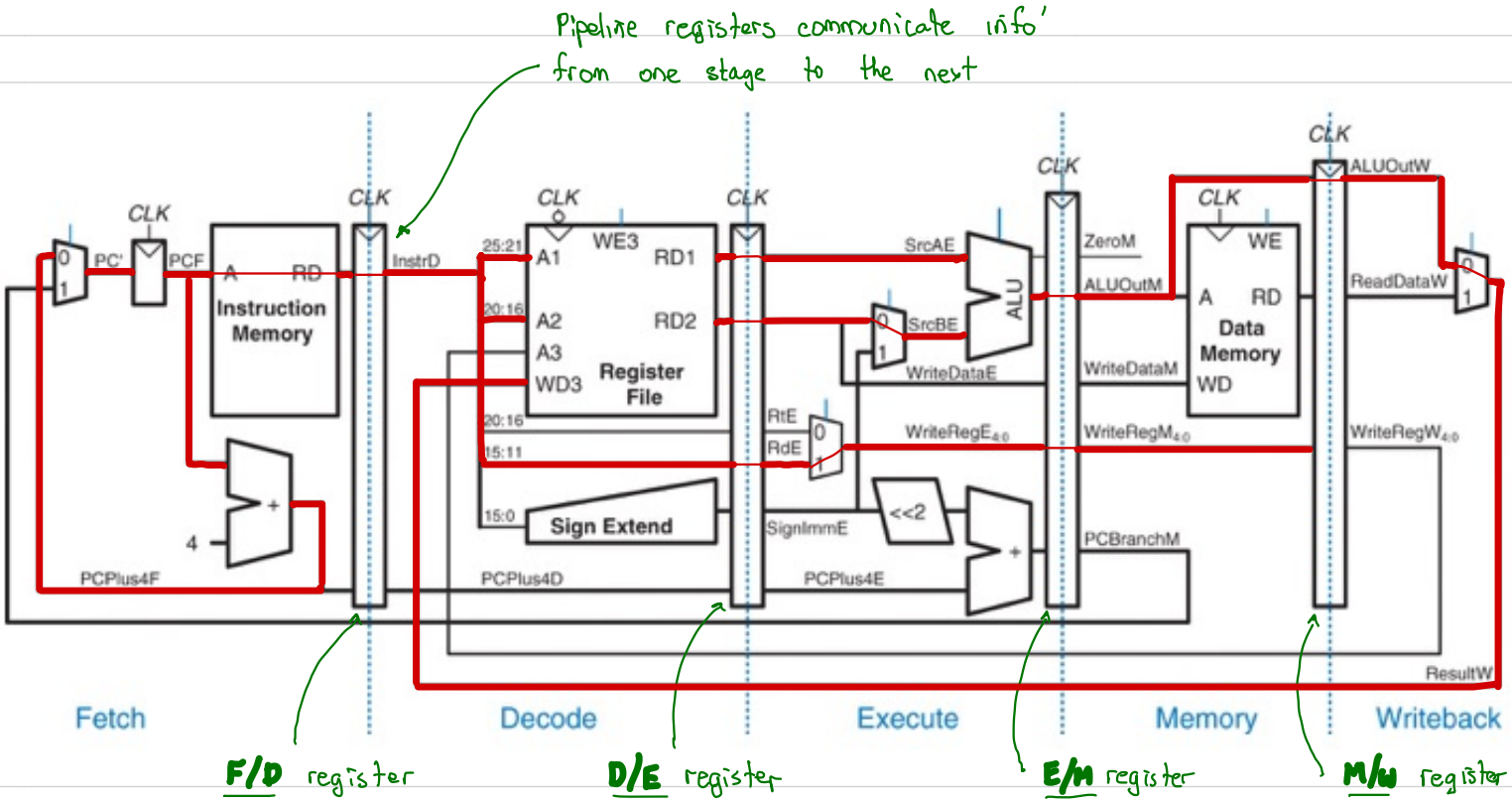
Pipeline registers (continued)

Pipelining is made possible by using more DFFs to make pipeline registers.

- more than 32 bits
- updates made on positive clock edges.

The processor now fitted with pipeline registers (Textbook Fig. 7.46)



Tracing the main datapath of an R-type instruction

Tracing an R-type instruction – details

Suppose we have

Address : 0x0040_0030 slt $2, $4, $5
(rd) (rs) (rt)

Fetch stage

Data written to the F/D register

- 32-bit instruction word for slt
- PC + 4 (0x0040_0034) written to PCPlus4F

Register syntax: PCPlus4F

PCPlus4F: name of the pipeline register field; stage (Fetch)

CLOCK EDGE: Data written to the "F" side of F/D register now available on "D" side.

Decode stage

Data written to the D/E pipeline register:

Needed for R-type instructions:

- RD1 (contents of GPR $4)
- RD2 (contents of GPR $5)
- $Instr_{15:11}$ 00010_2 (GPR $2)

Not need, but still copied

- $Instr_{20:16}$ 00101_2 (GPR $5)
- Sign-extended 32-bit constant
- PCPlus4D 0x0040_0034

- this is information that might be needed for other instruction types, but not R-type.

Execute stage

Data written to the E/M stage:

Important for R-type:

- 32-bit ALUResult, and Zero
- $Instr_{15:11}$ 00010_2 (GPR $2), called WriteRegE

Not needed:

- PCBranch (branch destination)

Memory stage

Data written to M/W register:

- ALUOutM (ALUResult for slt)
- WriteRegM (00010_2, GPR $2)

} passed straight through the Memory stage

Not needed:

- Dmem's RD output

Writeback stage

Finally, after the clock edge that copies the "M" side to the "W" side:

- ResultW (= ALUResult) and WriteRegW given to R-file.
- Write to R-file occurs on the next NEGATIVE clock edge (one-half cycle after the main clock edge).

Pipelined control

Exactly the same control unit as the single-cycle machine.

Control signals are produced in the Decode stage

- appropriate signals proceed from stage to stage in step with each instruction.

E.g., for slt:

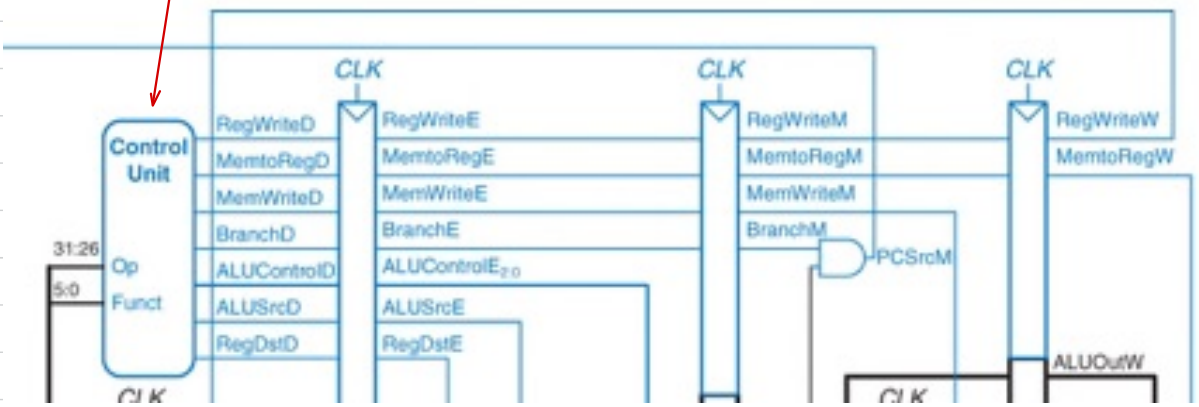
- Writeback controls are MemtoReg = 0, RegWrite = 1

- passed along through pipeline registers

D/E ⟶ E/M ⟶ M/W

↖ writeback control bits are not used until after storing in M/W register.

Control unit identical to single cycle machine



Control signals in "lock step" with data through each pipeline stage.