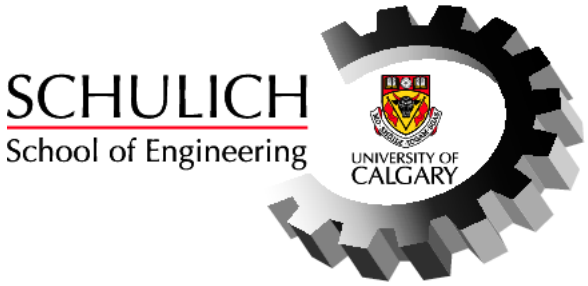

DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING

ENEL 353 - Digital Circuits

Final Examination

Tuesday, December 13, 2005
Auxiliary Gymnasium, 12:00 PM - 3:00 PM

L01 - Norm Bartley
L02 - Svetlana Yanushkevich

Instructions:

- Time allowed is 3 hours.
- The examination is closed-book.
- Non-programmable calculators are permitted.
- The maximum number of marks is 100, as indicated. Please attempt all questions.
- Please use a pen or heavy pencil to ensure legibility.
- If you use more than one examination booklet, please make sure that your name and ID number are on each.
- Where appropriate, marks will be awarded for proper and well-reasoned explanations.

---

1. [**8 marks.**] Use algebraic transformations to prove or disprove that the expressions given below for f and g are equal. (Do not use a truth table or Karnaugh map.)

$$f = (x' + y'(w'z)')' + wxz + w'$$
$$g = wxy \oplus wxz \oplus wxyz \oplus w \oplus 1$$

2. [**38 marks total.**] Consider the following two functions that are in terms of the four variables a, b, c, d:

$$f = \sum m(0, 1, 2, 6, 8, 10, 11, 12)$$
$$g = \sum m(0, 1, 2, 6, 7, 8, 10, 11, 12, 13)$$

Where appropriate in the questions below, you may assume that the system variables are available to your circuits in both complemented and uncomplemented forms.

(a) [**8 marks**] Draw Karnaugh maps and find minimal SOP and POS forms for each function.

(b) [**4 marks.**] Using your answer to part (a), implement the circuit for the function f using only 2-input NAND gates (inverters are not available). Appropriately choose the SOP or POS form in part (a) that yields the simplest circuit.

(c) [**4 marks.**] Using your answer to part (a), implement the circuit for the function g using only 2-input NOR gates (inverters are not available). Appropriately choose the SOP or POS form in part (a) that yields the simplest circuit.

(d) [**8 marks.**] Implement both functions using a PLA. Try to come up with the simplest-possible solution.

(e) [**4 marks.**] Implement both functions using a ROM.

(f) [**4 marks.**] Design the circuit for the function f using 3-to-8 decoders and any additional combinational gates that you may need. The decoders have enable inputs.

(g) [**6 marks.**] Design the circuit for the function g using 4-to-1 multiplexers. No other combinational gates are available.

3. **[20 marks total.]** Consider the 3-bit synchronous counter shown below in Fig. 1.

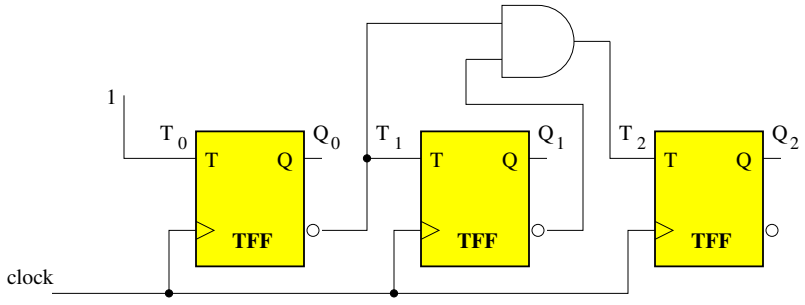

Fig. 1. Analyze this circuit

(a) **[12 marks.]** Derive the state table and the state diagram for this circuit and determine the sequence in which this counter counts. Treat Q_2 as the most-significant bit (MSB).

(b) **[8 marks.]** Redesign the system using D flip-flops.

4. **[34 marks total.]** Design a sequential circuit for a three-number combination lock. The circuit has three inputs w, x, y, and a single output z. The lock is opened by giving a series of three-bit binary codes on the system inputs w, x, y. The correct sequence is: $wxy = 010$, 100, 110 (this is the combination to the lock).

   Operation of the lock is as follows: Beginning in the "closed" state, entering the code $wxy = 001$ moves the system to the "1/3-open" state. From there, the next code $wxy = 101$ moves the system to the "2/3-open" state, but any other entry moves it back to closed. From 2/3-open, the final code $wxy = 011$ moves the system to the "open" state (and any other entry moves it to closed). When in the open state, the system should generate an output $z = 1$ (which controls a mechanical system that opens the lock). Finally, the system automatically (for any entry) moves to the closed state.

   (a) **[6 marks.]** Derive the state diagram for a Moore-type system. Use whatever you determine in this step for parts (b)-(d).

   (b) **[8 marks.]** Assign the necessary number of bits (for example, using variable names A and B) to represent the states of the system. Create the state table that defines the three input variables w, x, y, the current-states, next-states, and output z.

   (c) **[8 marks.]** Implement the system using D flip-flops and whatever combinational gates you may need, and sketch the circuit. *(Hint: Don't be surprised if you find no way to significantly simplify the functions!)*

   (d) **[10 marks.]** Using the method of your choosing, redesign the flip-flop input equations for JK flip-flops, and sketch the circuit.

   (e) **[2 marks.]** A very simple alternative way to implement the system with JK flip-flops is to replace each D flip-flop in part (c) directly with a JK flip-flop. Show how a JK flip-flop can be wired to emulate the behavior of a D flip-flop.
