Name: _____

ID#: _____

SCHULICH School of Engineering

UNIVERSITY OF CALGARY

DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING

ENEL 353 - Digital Circuits

Fall 2015 Final Examination

Course instructors: Norm Bartley and Steve Norman

Saturday, December 19, 2015
Time: 8:00 AM – 11:00 AM
Locations: ICT 121 and ICT 122

Instructions:

- Time allowed is 3 hours.
- Please review the examination rules on Page 2.
- You may use a calculator, but it must be one of the following sanctioned Schulich School of Engineering models: Casio FX-260, Casio FX-300MS, TI-30XIIS.
- The maximum number of marks is 94, as indicated. The final examination counts toward 50% of the final grade. Please attempt all questions.
- Please use a pen or heavy pencil to ensure legibility.
- Please answer questions in the spaces provided; if space is insufficient, please use the back of the pages.
- Where appropriate, marks will be awarded for proper and well-reasoned explanations.

(Please do not write in this space.)

1 *(17)*	**2** *(11)*	**3** *(12)*	**4** *(12)*	**5** *(9)*	**6** *(13)*	**7** *(8)*	**8** *(12)*	**Total** *(94)*

Student Identification

Each candidate must sign the Seating List confirming presence at the examination. All candidates for final examinations are required to place their University of Calgary I.D. cards on their desks for the duration of the examination. (Students writing mid-term tests can also be asked to provide identity proof.) Students without an I.D. card who can produce an **acceptable** alternative I.D., e.g., one with a printed name and photograph, are allowed to write the examination.

A student without acceptable I.D. will be required to complete an Identification Form. The form indicates that there is no guarantee that the examination paper will be graded if any discrepancies in identification are discovered after verification with the student's file. **A student who refuses to produce identification or who refuses to complete and sign the Identification Form is not permitted to write the examination.**

Examination Rules

(1) Students late in arriving will not normally be admitted after one-half hour of the examination time has passed.
(2) No candidate will be permitted to leave the examination room until one-half hour has elapsed after the opening of the examination, nor during the last 15 minutes of the examination. All candidates remaining during the last 15 minutes of the examination period must remain at their desks until their papers have been collected by an invigilator.
(3) All inquiries and requests must be addressed to supervisors only.
(4) **The following is strictly prohibited:**
    (a) speaking to other candidates or communicating with them under any circumstances whatsoever;
    (b) bringing into the examination room any textbook, notebook or document not authorized by the examiner;
    (c) making use of calculators, cameras, cell-phones, computers, headsets, pagers, PDA's, or any device not authorized by the examiner;
    (d) leaving examination papers exposed to view;
    (e) attempting to read other student's examination papers.

    The penalty for violation of these rules is suspension or expulsion or such other penalty as may be determined.
(5) Candidates are requested to write on both sides of the page, unless the examiner has asked that the left hand page be reserved for rough drafts or calculations.
(6) Discarded matter is to be struck out and not removed by mutilation of the examination answer book.
(7) Candidates are cautioned against writing on their examination paper any matter extraneous to the actual answering of the question set.
(8) The candidate is to write his/her name on each answer book as directed and is to number each book.
(9) During the examination a candidate must report to a supervisor before leaving the examination room.
(10) Candidates must stop writing when the signal is given. Answer books must be handed to the supervisor-in-charge promptly. Failure to comply with this regulation will be cause for rejection of an answer paper.
(11) If during the course of an examination a student becomes ill or receives word of a domestic affliction, the student should report at once to the supervisor, hand in the unfinished paper and request that it be cancelled. If physical and/or emotional ill health is the cause, the student must report at once to a physican/counsellor so that subsequent application for a deferred examination is supported by a completed Physician/Counsellor Statement form. Students can consult professionals at University Health Services or Counselling and Student Development Centre during normal working hours or consult their physician/counsellor in the community. **Once an examination has been handed in for marking a student cannot request that the examination be cancelled for whatever reason. Such a request will be denied. Retroactive withdrawals will also not be considered.**

1. **[17 marks total.]** *Numbers, codes and binary addition.*

   (a) **[2 mark.]** In *unsigned binary* format, the 12-bit pattern 100100100110 represents a certain integer. Express its value in Binary Coded Decimal (BCD) format.

   (b) **[2 marks.]** In *sign/magnitude* format, the eight-bit pattern 10011101 represents a certain integer. What is the eight-bit two's complement representation of the same integer?

   (c) **[3 marks.]** Convert the *hexadecimal* number $1B72_{16}$ to each of the formats given below. Show how you obtained your answers.

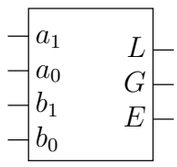
   octal: **decimal:**

   (d) **[2 marks.]** Use repeated division to find the octal representation of 2015_{10}.

   (e) **[1 mark.]** Convert the six-bit Gray code 110011 to unsigned binary code.

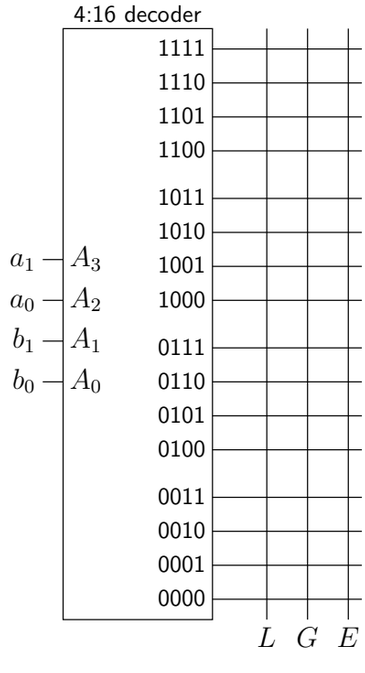
   (f) **[3 marks.]** Suppose that the 8-bit binary numbers 11011011 and 00101011 are added using 8-bit binary addition. If all numbers are interpreted as *unsigned*, will an overflow occur? If instead all numbers are interpreted as *two's-complement*, will an overflow occur? Give reasons for your answers.

   (g) **[4 marks.]** Consider building a 2-bit signed integer comparator, with inputs and outputs as shown to the right. $a_{1:0}$ and $b_{1:0}$ are two-bit *two's-complement* numbers. L is true if and only if (iff) $a_{1:0} < b_{1:0}$. Likewise, G is true iff $a_{1:0} > b_{1:0}$. Finally, E is true iff $a_{1:0}$ and $b_{1:0}$ are equal.



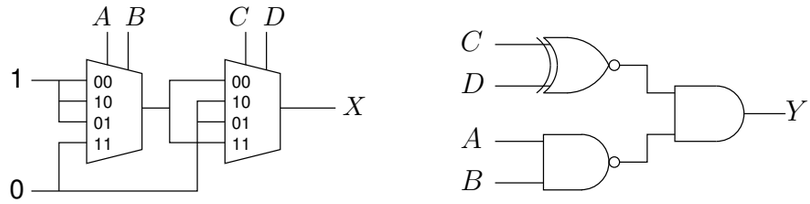
   Complete the truth table below, and use dot notation on the given ROM array to show how to implement the comparator as a ROM.

a_1	a_0	b_1	b_0	L	G	E
0	0	0	0			
0	0	0	1			
0	0	1	0			
0	0	1	1			
0	1	0	0			
0	1	0	1			
0	1	1	0			
0	1	1	1			
1	0	0	0			
1	0	0	1			
1	0	1	0			
1	0	1	1			
1	1	0	0			
1	1	0	1			
1	1	1	0			
1	1	1	1			



2. **[11 marks total.]** *Boolean algebra and multiplexers.*

   (a) **[4 marks.]** Use algebra to prove or disprove that $X(A, B, C, D) = Y(A, B, C, D)$ in the circuits shown below. Do not use a truth table or K-map.



   (b) **[4 marks.]** A useful property involving XOR operations is given by

$$A + B = A \oplus B \oplus AB.$$

   Prove this algebraically. Do not use a truth table or a K-map.

   (c) **[3 marks.]** Without using a truth table of a K-map, algebraically determine the minimal SOP form of the following expression:

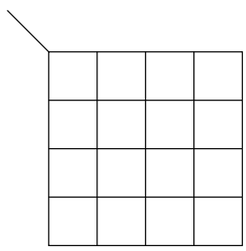
$$\overline{A}C\overline{D} + \overline{C}D + ABD + B\overline{C}D + \overline{(A + C + D)} + ABCD.$$

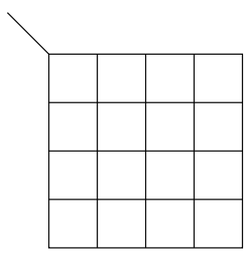
3. **[12 marks total.]** *K-map problems.*

   (a) **[7 marks.]** Consider the following two logic functions given in minterm and maxterm notation with the given don't-care conditions:

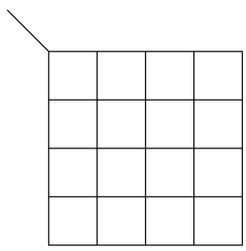
Function	**Expression**	**Don't-care cells**
$X(A,B,C,D)$	$\sum(m_0, m_2, m_4, m_5, m_6, m_7, m_9, m_{10})$	$3, 8, 13, 15$
$Y(A,B,C,D)$	$\prod(M_0, M_3, M_5, M_8, M_{14})$	$1, 12, 15$

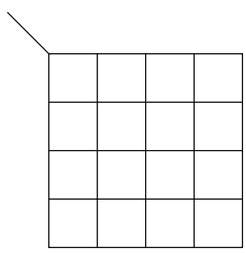
   Use the blank K-maps below to determine *all* minimal SOP expressions for each of X and Y. On just the map for X, indicate all of the distinguished 1-cells and the essential prime implicants. (You are welcome to draw extra K-maps to help present your solutions.)





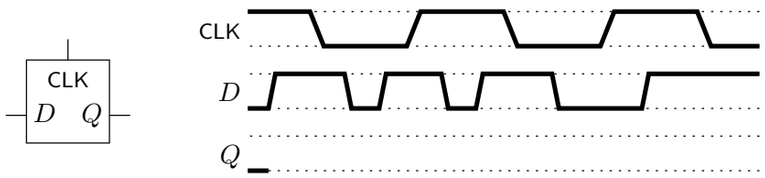
   (b) **[5 marks.]** Use the same maps from part (a) to determine *all* minimal POS expressions for each of X and Y.



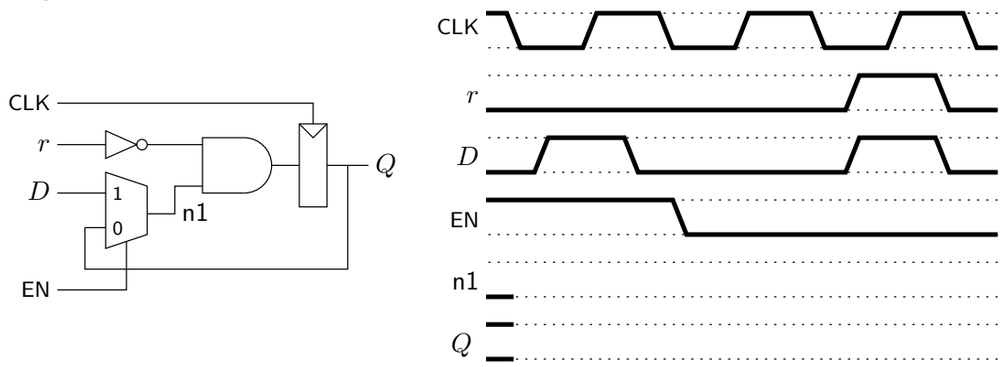


4. **[12 marks total.]** *Questions about sequential logic elements.*

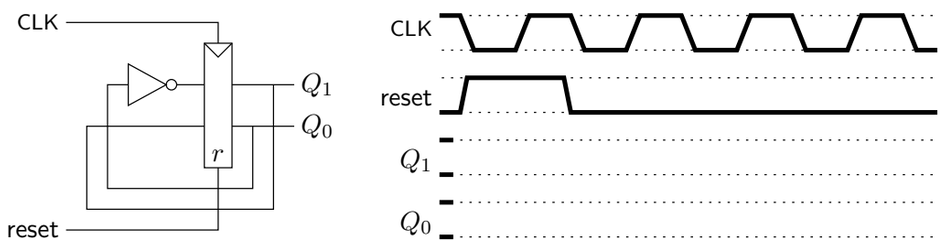
(a) **[3 marks.]** This part is about the essential behaviour of a D latch. Complete the timing diagram.



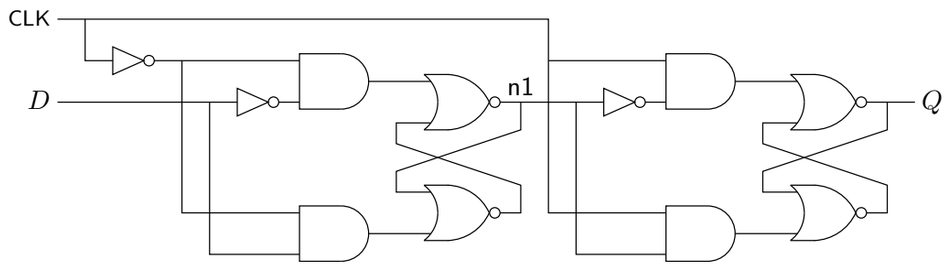
(b) **[3 marks.]** The schematic below shows one way to build a DFF (D flip-flop) with both an enable (EN) input and a synchronous reset (r) input, using a "plain" DFF and some combinational logic. Complete the timing diagram.



(c) **[3 marks.]** The state register in this circuit has synchronous reset. Complete the timing diagram.



(d) **[3 marks.]** The circuit below is a D flip-flop made from two D latches; each D latch uses a NOR-based SR latch. Use the given timing data to determine t_{pcq} and t_{ccq} for the D flip-flop.



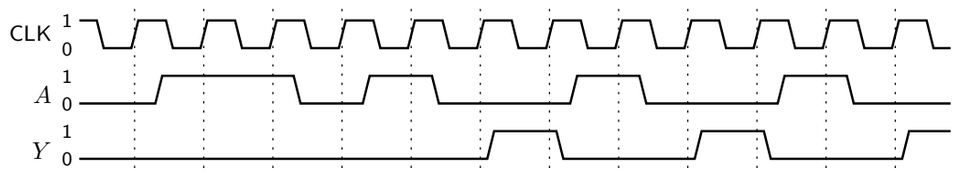
Important hints ... (1) You may assume that the signal on D satisfies a setup-time constraint, so that the signal at n1 is always stable well in advance of a rising edge of CLK. (2) You need to consider both possible cases in which n1 $\neq Q$ just before a rising edge of CLK.

gate	t_{pd}	t_{cd}
NOT	15 ps	10 ps
AND2	41 ps	32 ps
NOR2	33 ps	26 ps

5. **[9 marks total.]** Consider the design of an FSM with a 1-bit input A and a 1-bit output Y, with this behaviour ...

   - Y should be 1 if the FSM has detected the following values for A at the last 5 rising edges of CLK: from least-recent to most-recent, 11010.
   - Y should be 1 if the FSM has detected 11010 followed by one or more repetitions of the sequence 010.
   - Y should be 0 at all other times.

   In other words, the FSM detects 11010, 11010 010, 11010 010 010, and so on, as shown in this timing diagram:



   (a) **[1 mark.]** Should this be a Moore FSM design or a Mealy FSM design? Give a reason for your answer.

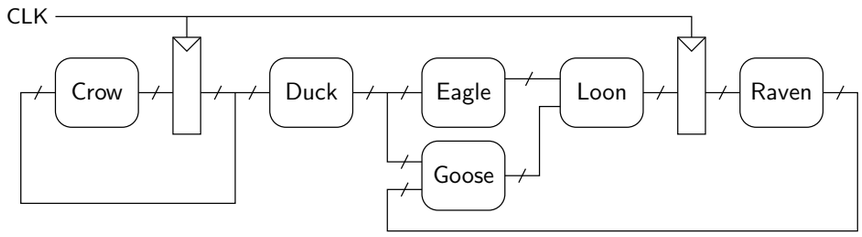
   (b) **[4 marks.]** Draw a state-transition diagram for the FSM.

   (c) **[4 marks.]** Make next-state and output logic tables that match the diagram of part (b). Use symbols such as S0, S1, and so on for the states.

6. **[13 marks total.]** *Questions about timing constraints and voltage levels.*

(a) **[4 marks.]** In the circuit below, timing parameters for the registers are: $t_{\text{setup}} = 51\,\text{ps}$, $t_{\text{hold}} = 12\,\text{ps}$, $t_{\text{pcq}} = 53\,\text{ps}$, and $t_{\text{ccq}} = 26\,\text{ps}$. Timing parameters for combinational logic are given in this table:

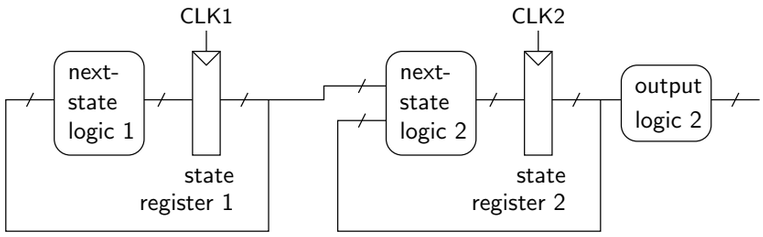
element	Crow	Duck	Eagle	Goose	Loon	Raven
t_{pd}, in ps	200	50	54	65	100	60
t_{cd}, in ps	37	25	25	25	75	40



Suppose that $t_{\text{skew}} = 21\,\text{ps}$. What is the minimum clock period T_{C} needed to ensure that there won't be a setup time violation?

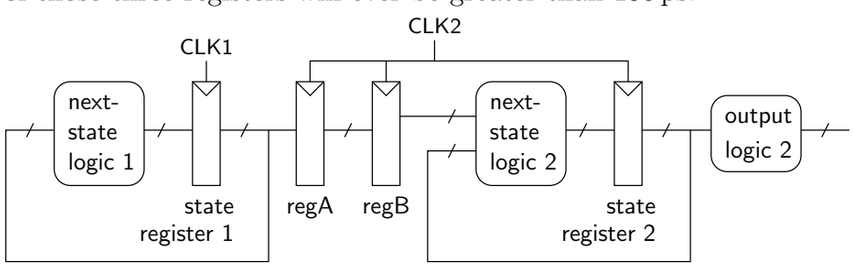
(b) **[2 marks.]** Now suppose that for the circuit of part (a), the value of t_{skew} is 60 ps. Is there a risk of a hold-time violation, or not? Provide numerical calculations to support your answer.

(c) **[2 marks.]** In the circuit below, CLK1 is expected to have a frequency of 90–100 MHz and CLK2 is expected to have a frequency of 2.9–3.0 GHz; the two clocks will come from completely unrelated sources. The element called next-state logic 1 has been designed to avoid any timing problems on the path from state register 1 back to state register 1; similarly, next-state logic 2 has been designed to avoid any timing problems on the path from state register 2 back to state register 2.



Explain briefly why there is a major risk of metastability in state register 2.

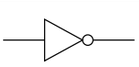
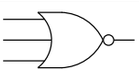
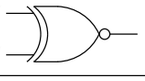
(d) **[2 marks.]** Suppose that the circuit of part (c) is redesigned as shown below, and that t_{setup} for each of regA, regB, and state register 2 is 40 ps. Suppose also that it is extremely unlikely that the resolution time for each of those three registers will ever be greater than 150 ps.



Explain briefly why there is no longer a major risk of metastability in state register 2.

(e) **[3 marks.]** The table below on the left specifies important voltage levels for the Advanced High Speed TTL-Compatible CMOS logic family operating with $V_{\text{DD}} = 5.0\,\text{V}$. Fill in the table on the right with either the most precise possible range of output voltages, or an explanation of why the range is unknown.

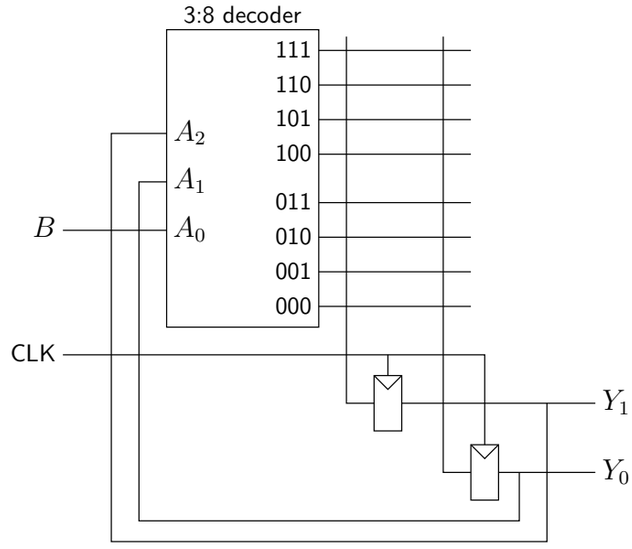
V_{OH}	3.80 V
V_{IH}	2.00 V
V_{IL}	1.35 V
V_{OL}	0.44 V

gate	output range or explanation
	
	
	

7. **[8 marks total.]** *Design of synchronous counters.*

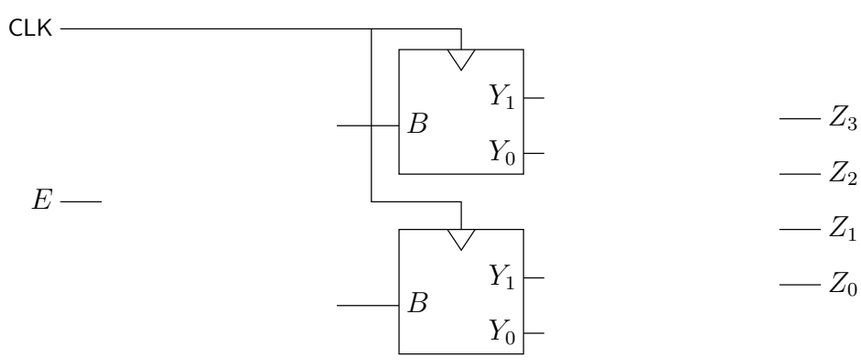
(a) **[4 marks.]** Consider the design of a counter with 1-bit input B and a two-bit output $Y_{1:0}$. When $B = 1$ the output should go through the cycle 00, 01, 10, 11, 00, 01, and so on, changing on each rising edge of CLK. When $B = 0$ the output should stay frozen from one clock cycle to the next.

Such a counter can be built with a small ROM array and two DFFs. Put dots on the ROM array to complete the design, using the space to the right of the schematic to show your intermediate steps.



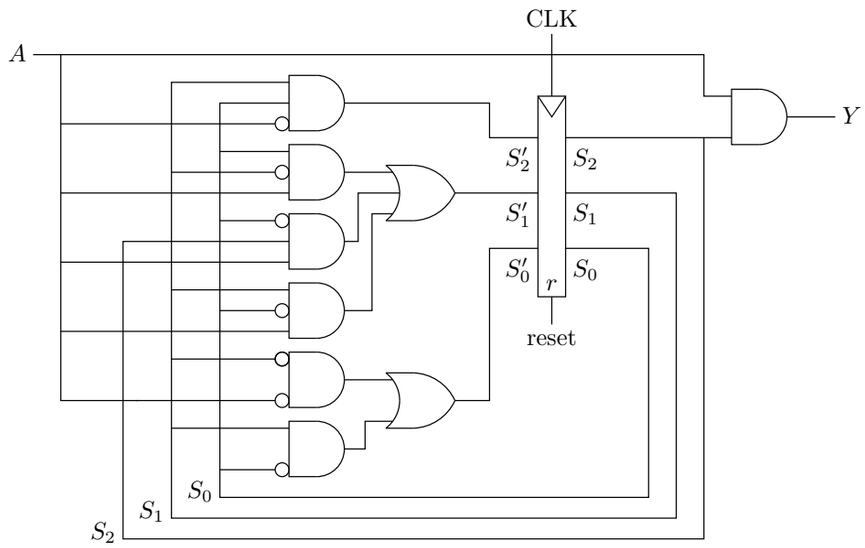
(b) **[4 marks.]** Now consider the design of a similar counter, with 1-bit input E and four-bit output $Z_{3:0}$. When $E = 0$, the counter should be frozen, and when $E = 1$, the counter should cycle through the unsigned binary sequence 0000, 0001, 0010, ..., 1110, 1111, 0000, 0001, and so on.

The incomplete schematic below shows two copies of the counter designed in part (a), and the signals E and $Z_{3:0}$. By adding one or two logic gates and some wires, complete the design of the counter described in the previous paragraph, then write one or two short sentences to explain how the design works.



8. **[12 marks total.]** *Questions about FSM analysis.*

(a) **[8 marks.]** Consider the FSM sketched below. There is one input A, and one output Y. Determine the combined state and output table, and sketch the state-transition diagram. In your tables, use 0's and 1's for the states and next states, not symbols like S0, S1, etc.



(b) **[4 marks.]** Below is the combined state and output table for a FSM that has one input A, and one output Y. The state variables are $S_{2:0}$. Use this table to complete the timing diagram.

$S_{2:0}$	A	$S'_{2:0}$	Y	$S_{2:0}$	A	$S'_{2:0}$	Y
000	0	000	0	010	1	001	0
000	1	001	0	011	0	100	0
001	0	010	1	011	1	011	0
001	1	011	1	100	0	000	1
010	0	000	0	100	1	001	1