1XB
S.N.
S.Y.

Name: _____

ID#: _____

Section: _____

(L01 was with N. Bartley in ST 145; L02 was with S. Norman in ENE 243.)

SCHULICH School of Engineering

UNIVERSITY OF CALGARY

DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING

ENEL 353 - Digital Circuits

Fall 2016 Final Examination

Course instructors: Norm Bartley and Steve Norman

Monday, December 12, 2016
Start Time: 3:30 PM
Locations: ICT 102 (L01), ICT 121 (L02)

Instructions:

- Time allowed is 3 hours.
- Please review the examination rules on Page 2.
- You may use a calculator, but it must be one of the following sanctioned Schulich School of Engineering models: Casio FX-260, Casio FX-300MS, TI-30XIIS.
- The maximum number of marks is 97, as indicated. The final examination counts toward 50% of the final grade. Please attempt all questions.
- Please use a pen or heavy pencil to ensure legibility.
- Please answer questions in the spaces provided; if space is insufficient, please use the back of the pages.
- Where appropriate, marks will be awarded for proper and well-reasoned explanations.

(Please do not write in this space.)

1 *(14)*	**2** *(8)*	**3** *(11)*	**4** *(13)*	**5** *(10)*	**6** *(10)*	**7** *(10)*	**8** *(9)*	**9** *(12)*	**Total** *(97)*

Student Identification

Each candidate must sign the Seating List confirming presence at the examination. All candidates for final examinations are required to place their University of Calgary I.D. cards on their desks for the duration of the examination. (Students writing mid-term tests can also be asked to provide identity proof.) Students without an I.D. card who can produce an **acceptable** alternative I.D., e.g., one with a printed name and photograph, are allowed to write the examination.

A student without acceptable I.D. will be required to complete an Identification Form. The form indicates that there is no guarantee that the examination paper will be graded if any discrepancies in identification are discovered after verification with the student's file. **A student who refuses to produce identification or who refuses to complete and sign the Identification Form is not permitted to write the examination.**

Examination Rules

(1) Students late in arriving will not normally be admitted after one-half hour of the examination time has passed.

(2) No candidate will be permitted to leave the examination room until one-half hour has elapsed after the opening of the examination, nor during the last 15 minutes of the examination. All candidates remaining during the last 15 minutes of the examination period must remain at their desks until their papers have been collected by an invigilator.

(3) All inquiries and requests must be addressed to supervisors only.

(4) **The following is strictly prohibited:**

   (a) speaking to other candidates or communicating with them under any circumstances whatsoever;
   (b) bringing into the examination room any textbook, notebook or document not authorized by the examiner;
   (c) making use of calculators, cameras, cell-phones, computers, headsets, pagers, PDA's, or any device not authorized by the examiner;
   (d) leaving examination papers exposed to view;
   (e) attempting to read other student's examination papers.

   The penalty for violation of these rules is suspension or expulsion or such other penalty as may be determined.

(5) Candidates are requested to write on both sides of the page, unless the examiner has asked that the left hand page be reserved for rough drafts or calculations.

(6) Discarded matter is to be struck out and not removed by mutilation of the examination answer book.

(7) Candidates are cautioned against writing on their examination paper any matter extraneous to the actual answering of the question set.

(8) The candidate is to write his/her name on each answer book as directed and is to number each book.

(9) During the examination a candidate must report to a supervisor before leaving the examination room.

(10) Candidates must stop writing when the signal is given. Answer books must be handed to the supervisor-in-charge promptly. Failure to comply with this regulation will be cause for rejection of an answer paper.

(11) If during the course of an examination a student becomes ill or receives word of a domestic affliction, the student should report at once to the supervisor, hand in the unfinished paper and request that it be cancelled. If physical and/or emotional ill health is the cause, the student must report at once to a physican/counsellor so that subsequent application for a deferred examination is supported by a completed Physician/Counsellor Statement form. Students can consult professionals at University Health Services or Counselling and Student Development Centre during normal working hours or consult their physician/counsellor in the community. **Once an examination has been handed in for marking a student cannot request that the examination be cancelled for whatever reason. Such a request will be denied. Retroactive withdrawals will also not be considered.**

1. **[14 marks total.]** *Questions about integer representation and arithmetic.*

   (a) **[3 marks.]** (Give all answers to this part in base ten.) Consider the 12-bit pattern 1001 0100 0101.

   What number does it represent in a 12-bit unsigned binary system?

   What number does it represent in a 12-bit sign-magnitude system?

   What number does it represent in a 12-bit BCD system?

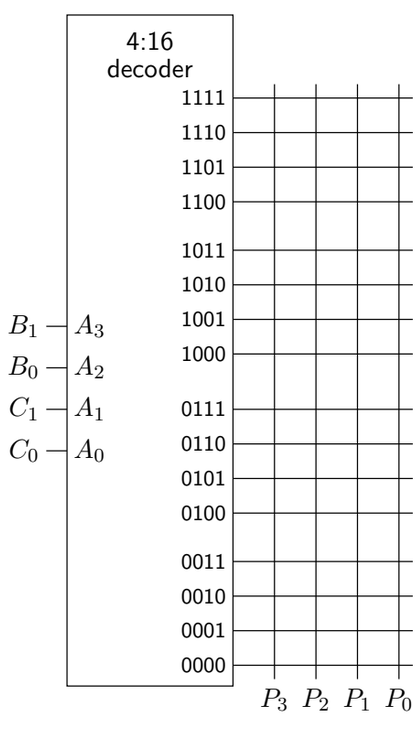
   (b) **[2 marks.]** What number does 1110 0101 represent in an 8-bit two's-complement system? Give your answer in base ten.

   (c) **[2 marks.]** Use repeated division to convert 389_{10} to octal represention.

   (d) **[3 marks.]** Compute the results (sum and overall carry-out) of the 6-bit addition $111011_2 + 010001_2$. Then give

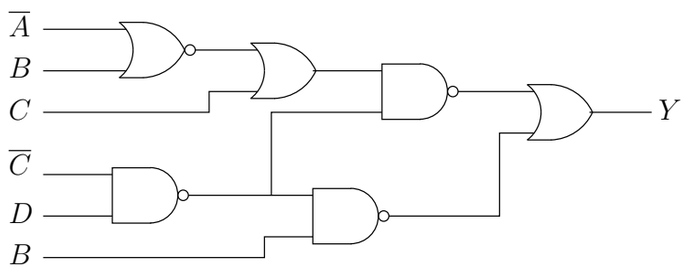
   - a yes/no answer about unsigned overflow, with a reason;
   - a yes/no answer about signed overflow, with a reason.

   (e) **[4 marks.]** Put dots on the ROM array to implement a circuit that computes the result of multiplying two 2-bit unsigned integers. For example, $B_{1:0} = 10$ and $C_{1:0} = 11$, then $P_{3:0}$ should be 0110, because $2 \times 3 = 6$..



2. **[8 marks total.]** *Boolean algebra and multiplexers.*

   (a) **[5 marks.]** Use algebra and/or bubble-pushing to determine a minimal SOP expresseion for Y. Do not use a truth table or K-map.



   (b) **[3 marks.]** Without using a truth table of a K-map, algebraically determine the minimal SOP form of the following expression:

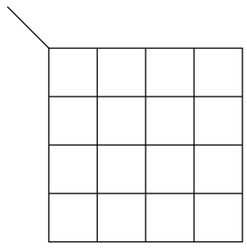
$$C \oplus B \oplus \overline{A} \oplus C$$

3. **[11 marks total.]** *K-map problems.*

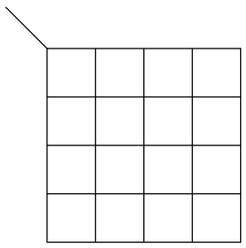
   (a) **[6 marks.]** Consider the logic functions $X(A, B, C, D)$ and $Y(A, B, C, D, E)$ given below as minterm lists:

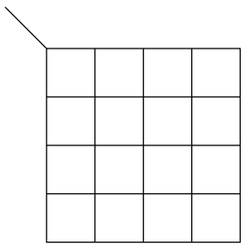
Function	**1-cells**	**Don't-care cells**
X	$5, 7, 9, 11, 13, 14$	$2, 6, 10, 12, 15$
Y	$4, 6, 8, 9, 12, 13, 17, 19, 20, 21, 22, 23, 26, 27, 30$	$16, 24, 28$

   Use the blank K-map below to determine *all* minimal SOP expressions for X. Indicate all of the distinguished 1-cells and the essential prime implicants. (You are welcome to draw extra K-maps to help present your solutions.)



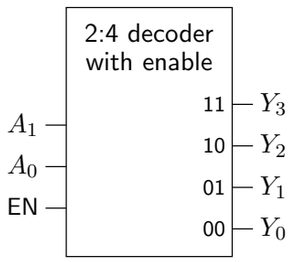
   (b) **[5 marks.]** Use the blank K-maps below to determine *all* minimal POS expressions for Y.

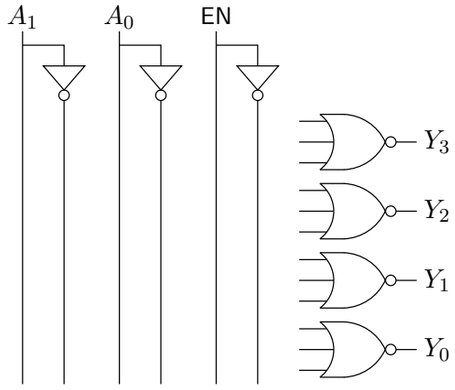




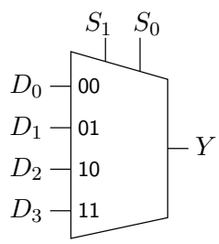
4. **[13 marks total.]** *Questions about multiplexers and decoders.*

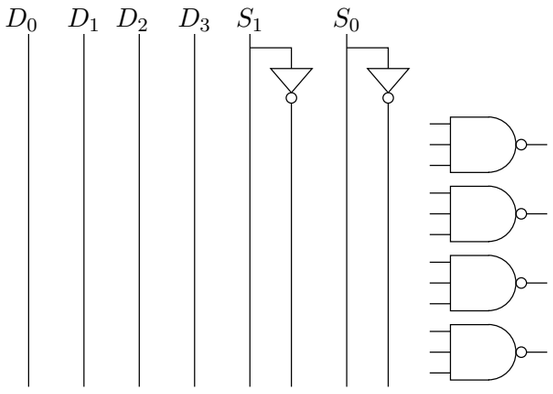
(a) **[3 marks.]** Below on the left is the symbol for a 2:4 decoder-with-enable. Add wires to the schematic below on the right to implement a 2:4 decoder-with-enable.





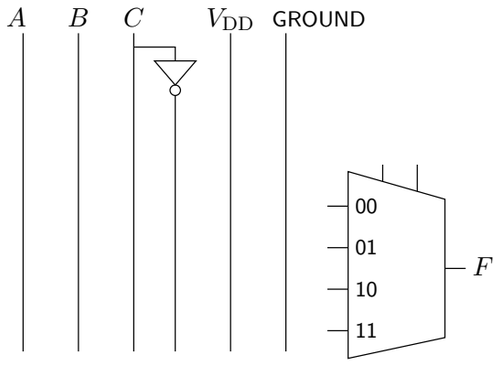
(b) **[3 marks.]** Below on the left is the symbol for a 4:1 multiplexer. Add *one additional logic gate* and some wires to the schematic below on the right to implement a 4:1 multiplexer.





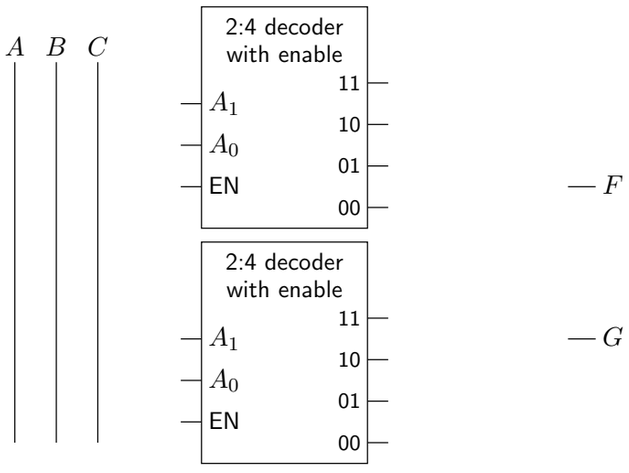
(c) **[3 marks.]** Add wires—*but no additional logic elements*—to implement the function given in the truth table.

A	B	C	F
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	1



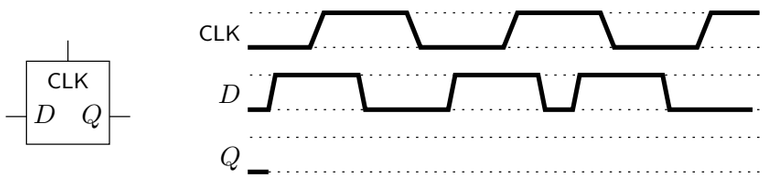
(d) **[4 marks.]** To the schematic given below, add wires, *one* NOT gate, and as many OR gates as you need to implement the functions F and G given in the truth table.

A	B	C	F	G
0	0	0	0	1
0	0	1	1	0
0	1	0	1	0
0	1	1	1	0
1	0	0	0	1
1	0	1	0	1
1	1	0	0	0
1	1	1	1	0



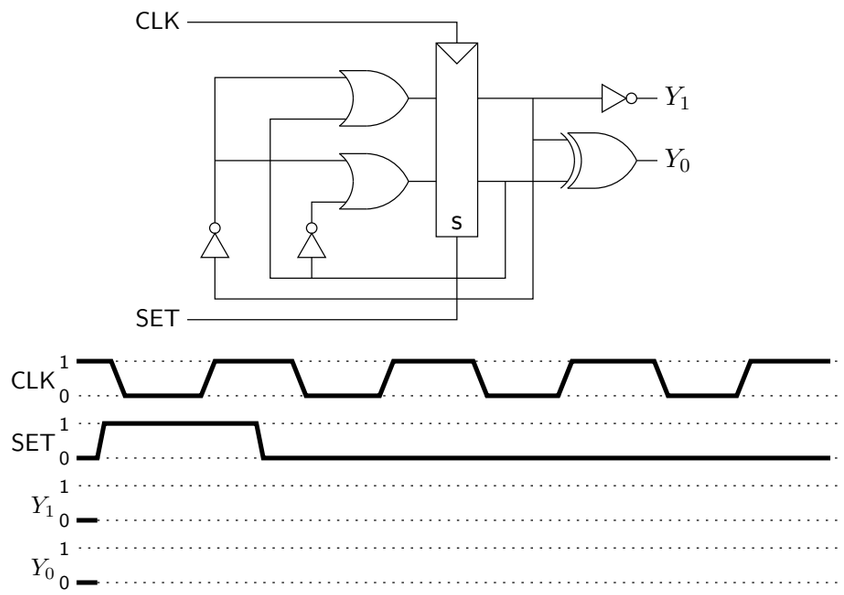
5. [**10 marks total.**] *Questions about sequential logic elements.*

(a) **[3 marks.]** This part is about the essential behaviour of a D latch. Complete the timing diagram.



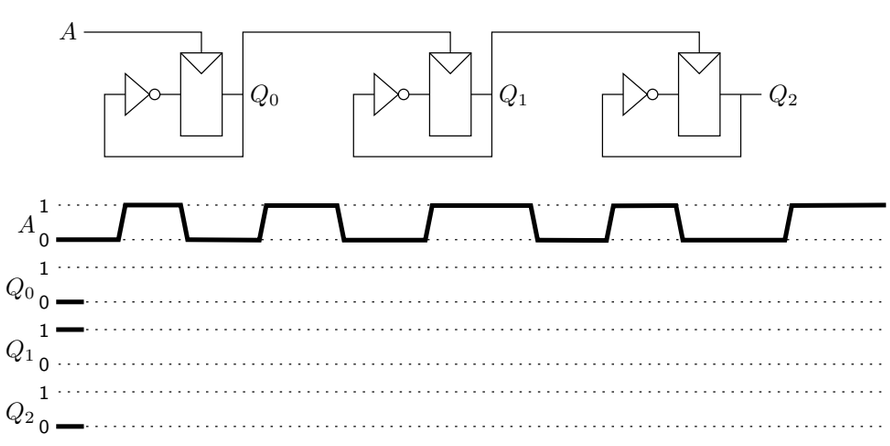
(b) **[4 marks.]** The 2-bit state register in the circuit below has a *synchronous* set input. Complete the timing diagram.

(Hint: There is room for rough work underneath the timing diagram.)



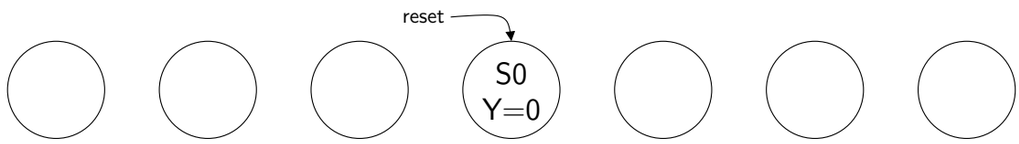
(c) **[3 marks.]** Normally the clock inputs of D flip-flops are connected to periodic clock signals. But the circuit below is an application of D flip-flops in which the clock inputs are not necessarily periodic.

Assume, as shown, that $Q_0 = 0$, $Q_1 = 1$, and $Q_2 = 0$ at the beginning of the time interval in the given timing diagram. Complete the timing diagram.



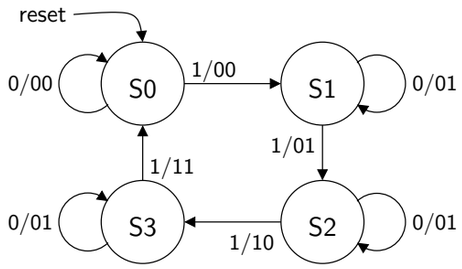
6. **[10 marks total.]** *Questions about FSM design.*

(a) **[4 marks.]** Consider the design of an FSM with a 1-bit input A and a 1-bit output Y. Y should be 1 if there have been at least three rising edges of the clock since the most recent reset, and the value of A has been the same the three most recent rising edges of the clock (either 0, 0, 0 or 1, 1, 1). Y should be 0 at all other times.



(b) **[6 marks.]** The FSM design in this part is *not related* to the design of part (a). There are a 1-bit input A and a 2-bit output $Y_{1:0}$.

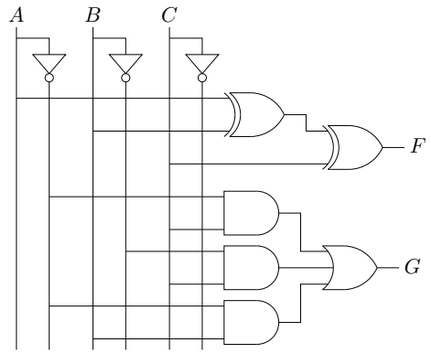
Using the state-transition diagram and state encoding given below, find minimal SOP expressions for next-state and output logic.



state	S_1	S_0
S0	0	0
S1	0	1
S2	1	1
S3	1	0

7. **[10 marks total.]** *Questions about timing in logic circuits.*

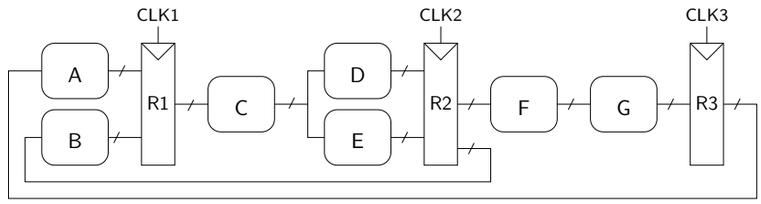
(a) **[3 marks.]** Consider the following circuit and timing parameters:



gate	t_{pd}	t_{cd}
NOT	30 ps	20 ps
AND2	62 ps	51 ps
OR3	76 ps	59 ps
XOR2	85 ps	56 ps

Find the overall t_{pd} and t_{cd} for the circuit, showing calculations that support your answer.

(b) **[3 marks.]** Consider this circuit built from 3 registers and 7 combinational elements.



In this part, assume that CLK1, CLK2, and CLK3 are identical signals—same period, with edges at exactly the same times. Timing parameters for the registers are: $t_{setup} = 30\,\text{ps}$, $t_{hold} = 12\,\text{ps}$, $t_{pcq} = 35\,\text{ps}$, $t_{ccq} = 21\,\text{ps}$.

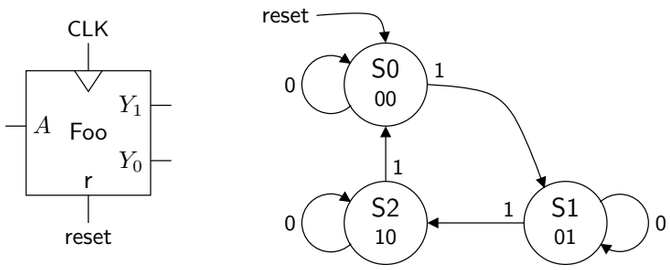
Find the minimum clock period T_C required for reliable operation of the circuit. Show calculations to support your answer.

element	t_{pd}	t_{cd}
A	202 ps	104 ps
B	210 ps	24 ps
C	82 ps	60 ps
D	133 ps	70 ps
E	100 ps	64 ps
F	90 ps	18 ps
G	75 ps	40 ps

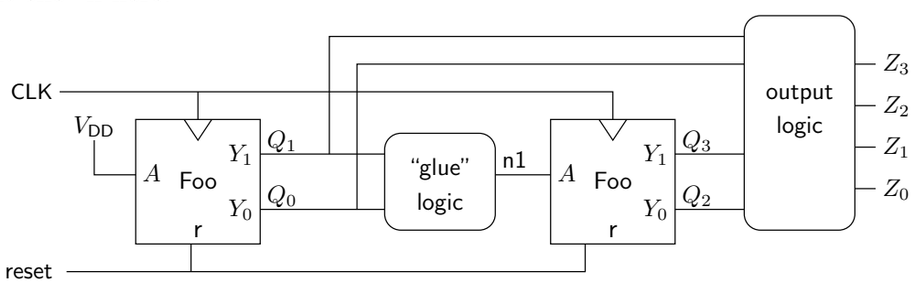
(c) **[4 marks.]** Consider the circuit of part (b) again, but this time assume that $T_C = 320\,\text{ps}$, and there is a non-zero clock skew t_{skew}. What is the largest allowable t_{skew} to avoid setup-time violation? And what is the largest allowable t_{skew} to avoid a hold-time violation?

8. **[9 marks total.]** *A problem in synchronous sequential logic design.*

The device labeled Foo in the diagram below is an FSM with the given state transition diagram.



Two of these devices are connected with some combinational logic to make the circuit shown here:



It's desired that the bit pattern $Z_{3:0}$ go to 0000 after reset, then cycle through 0001, 0010, 0011, ... , 1000, and back to 0000, updating one eaxh rising edge of CLK.

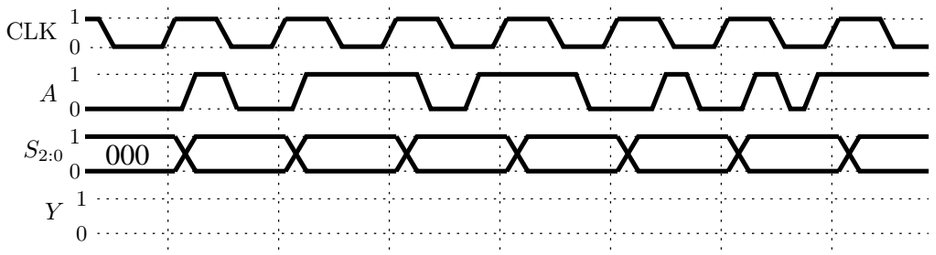
(a) **[2 marks.]** Write a Boolean algebra equation for the "glue" logic. Give a clear reason to support your answer.

(b) **[7 marks.]** Write four Boolean algebra equations for the output logic, using K-maps to ensure that the equations are in minimal SOP form.

9. **[12 marks total.]** *Questions about FSM analysis.*

(a) **[4 marks.]** Below is the combined state and output table for a FSM that has one input A, and one output Y. The state variables are $S_{2:0}$. Use this table to complete the timing diagram.

$S_{2:0}$	A	$S'_{2:0}$	Y	$S_{2:0}$	A	$S'_{2:0}$	Y
000	0	001	0	010	1	000	0
000	1	000	0	011	0	001	0
001	0	001	0	011	1	010	1
001	1	011	0	110	0	110	1
010	0	110	0	110	1	011	0



(b) **[8 marks.]** Consider the FSM sketched below. There is one input A, and one output Y. Determine the combined state and output table, and sketch the state-transition diagram. In your tables, use 0's and 1's for the states and next states, not symbols like S0, S1, etc.