Name: _____

ID#: _____

Section: _____

(L01 was with N. Bartley in ST 143; L02 was with S. Norman in ST 145.)

SCHULICH School of Engineering

UNIVERSITY OF CALGARY

DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING

ENEL 353 - Digital Circuits

Fall 2017 Final Examination

Course instructors: Norm Bartley and Steve Norman

Friday, December 15, 2017
Start Time: 7:00 PM
Location: KN GOLD

Instructions:

- Time allowed is 3 hours.
- Please review the examination rules on Page 2.
- You may use a calculator, but it must be one of the following sanctioned Schulich School of Engineering models: Casio FX-260, Casio FX-300MS, TI-30XIIS.
- The maximum number of marks is 104, as indicated. The final examination counts toward 50% of the final grade. Please attempt all questions.
- Please use a pen or heavy pencil to ensure legibility.
- Please answer questions in the spaces provided; if space is insufficient, please use the back of the pages.
- Where appropriate, marks will be awarded for proper and well-reasoned explanations.

(Please do not write in this space.)

1 *(16)*	**2** *(11)*	**3** *(11)*	**4** *(12)*	**5** *(10)*	**6** *(13)*	**7** *(11)*	**8** *(8)*	**9** *(12)*	**Total** *(104)*

Student Identification

Each candidate must sign the Seating List confirming presence at the examination. All candidates for final examinations are required to place their University of Calgary I.D. cards on their desks for the duration of the examination. (Students writing mid-term tests can also be asked to provide identity proof.) Students without an I.D. card who can produce an **acceptable** alternative I.D., e.g., one with a printed name and photograph, are allowed to write the examination.

A student without acceptable I.D. will be required to complete an Identification Form. The form indicates that there is no guarantee that the examination paper will be graded if any discrepancies in identification are discovered after verification with the student's file. **A student who refuses to produce identification or who refuses to complete and sign the Identification Form is not permitted to write the examination.**

Examination Rules

(1) Students late in arriving will not normally be admitted after one-half hour of the examination time has passed.

(2) No candidate will be permitted to leave the examination room until one-half hour has elapsed after the opening of the examination, nor during the last 15 minutes of the examination. All candidates remaining during the last 15 minutes of the examination period must remain at their desks until their papers have been collected by an invigilator.

(3) All inquiries and requests must be addressed to supervisors only.

(4) **The following is strictly prohibited:**

   (a) speaking to other candidates or communicating with them under any circumstances whatsoever;
   (b) bringing into the examination room any textbook, notebook or document not authorized by the examiner;
   (c) making use of calculators, cameras, cell-phones, computers, headsets, pagers, PDA's, or any device not authorized by the examiner;
   (d) leaving examination papers exposed to view;
   (e) attempting to read other student's examination papers.

   The penalty for violation of these rules is suspension or expulsion or such other penalty as may be determined.

(5) Candidates are requested to write on both sides of the page, unless the examiner has asked that the left hand page be reserved for rough drafts or calculations.

(6) Discarded matter is to be struck out and not removed by mutilation of the examination answer book.

(7) Candidates are cautioned against writing on their examination paper any matter extraneous to the actual answering of the question set.

(8) The candidate is to write his/her name on each answer book as directed and is to number each book.

(9) During the examination a candidate must report to a supervisor before leaving the examination room.

(10) Candidates must stop writing when the signal is given. Answer books must be handed to the supervisor-in-charge promptly. Failure to comply with this regulation will be cause for rejection of an answer paper.

(11) If during the course of an examination a student becomes ill or receives word of a domestic affliction, the student should report at once to the supervisor, hand in the unfinished paper and request that it be cancelled. If physical and/or emotional ill health is the cause, the student must report at once to a physican/counsellor so that subsequent application for a deferred examination is supported by a completed Physician/Counsellor Statement form. Students can consult professionals at University Health Services or Counselling and Student Development Centre during normal working hours or consult their physician/counsellor in the community. **Once an examination has been handed in for marking a student cannot request that the examination be cancelled for whatever reason. Such a request will be denied. Retroactive withdrawals will also not be considered.**

1. **[16 marks total.]** *Questions about number representations and arithmetic.*

   (a) **[2 marks.]** Convert the octal number 735204_8 to hexadecimal representation.

   (b) **[3 marks.]** Use repeated division to find the 8-bit unsigned binary representation of 37_{10}.

   (c) **[2 marks.]** Convert the 8-bit two's complement number 11110000_2 to decimal representation.

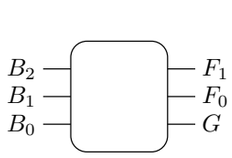
   (d) **[2 marks.]** Find the results (sum and carry-out-from-MSB) of the 5-bit binary addition $11001_2 + 11100_2$.

   (e) **[1 mark.]** If the numbers in the addition of part (d) are taken to be unsigned, was there overflow? Give a clear reason to support your answer.

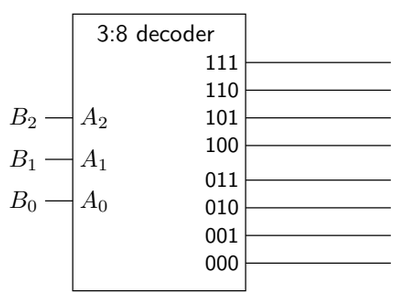
   (f) **[1 mark.]** If the numbers in the addition of part (d) are taken to be part of a two's-complement system, was there overflow? Give a clear reason to support your answer.

   (g) **[2 marks.]** Find the 12-bit BCD representation of the octal number 653_8.

   (h) **[3 marks.]** The table below specifies the behaviour of a 3-input, 3-output combinational element. In the table, N is the number $B_{2:0}$ represents in an unsigned binary system. Complete the diagram below on the right to show how the element can be implemented as a ROM array.

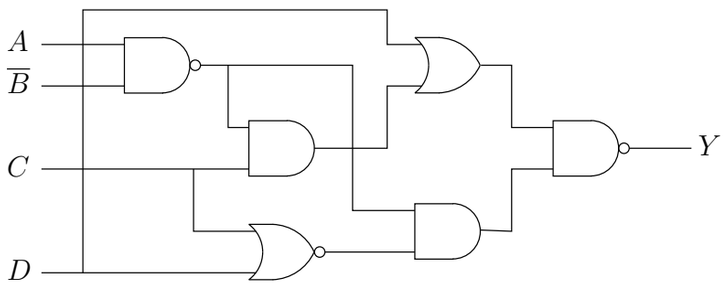


value of N	F_1	F_0	G
$N = 0$	0	0	1
$N = 1$	0	1	0
$2 \leq N < 4$	1	0	0
$N \geq 4$	1	1	0



2. **[11 marks total.]** *Questions on Boolean algebra.*

   (a) **[5 marks.]** Use algebra and/or bubble-pushing to determine a minimal SOP expresseion for Y. Do not use a truth table or K-map.



   (b) **[6 marks.]** Several key properties of Boolean algebra carry over directly to exclusive-OR (XOR) operations. Use algebraic manipulation and the definition of $A \oplus B$ as $\overline{A}\,B + A\,\overline{B}$ to prove the two properties given below. Do not use truth tables or K-maps.

      i. **Associativity:** $A \oplus (B \oplus C) = (A \oplus B) \oplus C$.

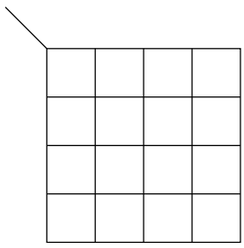
      ii. **Distributivity:** $A(B \oplus C) = AB \oplus AC$

3. **[11 marks total.]** *K-map problems.*

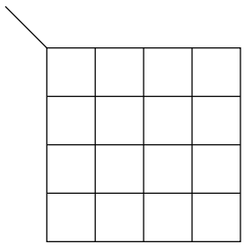
   (a) **[6 marks.]** Consider the logic functions $Y(A, B, C, D)$ and $Z(A, B, C, D)$ given below as minterm lists:

Function	**1-cells**	**Don't-care cells**
Y	$5, 6, 7, 11, 13, 14$	$3, 9, 10, 15$
Z	$4, 6, 9, 10, 11, 13$	$2, 12, 15$

   Use the blank K-map below to determine *all* minimal SOP expressions for Y. Indicate all of the distinguished 1-cells and the essential prime implicants. (You are welcome to draw extra K-maps to help present your solutions.)

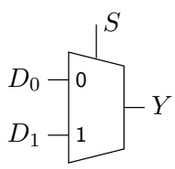


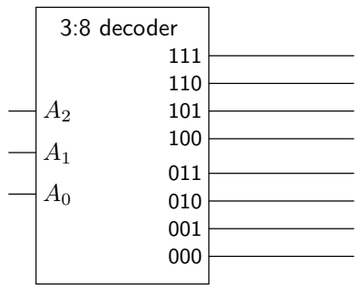
   (b) **[5 marks.]** Use the blank K-map below to determine *all* minimal POS expressions for Z.



4. **[12 marks total.]** *Questions about multiplexers and decoders.*

(a) **[4 marks.]** Below on the left is the symbol for a 2:1 multiplexer, and an 8x1 ROM array is shown on the right. Add wires and dots—*but no additional logic elements*—to the ROM array to implement a 2:1 multiplexer.

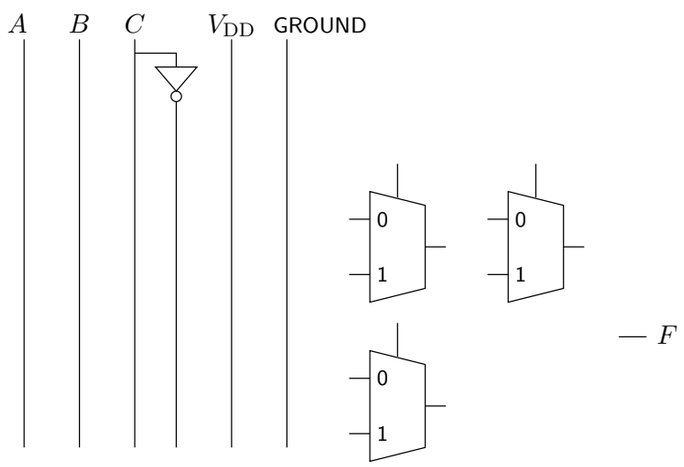




(b) **[1 mark.]** Determine the dimensions of the ROM array necessary to implement an 8:1 multiplexer.

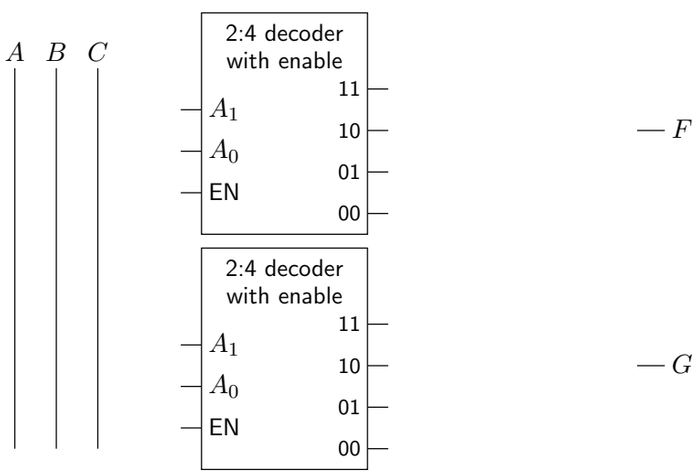
(c) **[3 marks.]** Add wires—*but no additional logic elements*—to implement the function given in the truth table.

A	B	C	F
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0



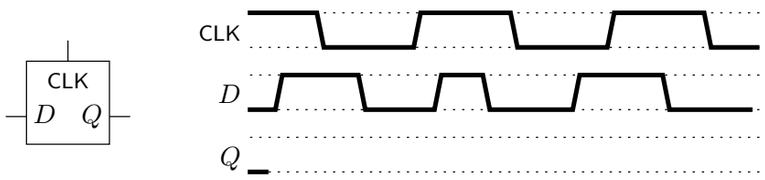
(d) **[4 marks.]** To the schematic given below, add wires, *one* NOT gate, and as many OR gates as you need to implement the functions F and G given in the truth table.

A	B	C	F	G
0	0	0	0	0
0	0	1	0	1
0	1	0	1	1
0	1	1	0	0
1	0	0	1	1
1	0	1	1	0
1	1	0	1	0
1	1	1	0	1

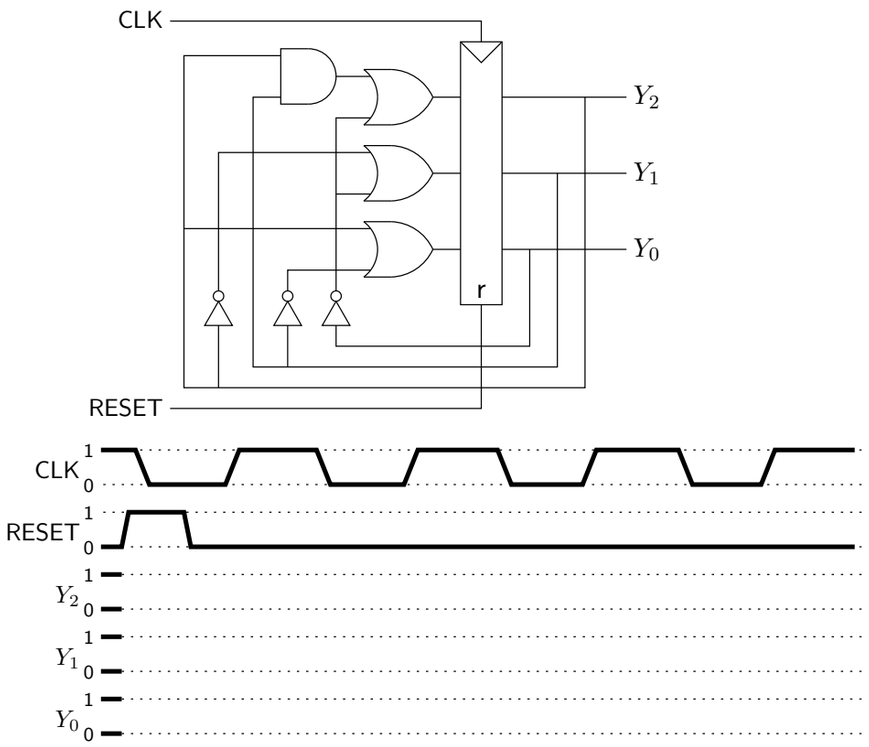


5. **[10 marks total.]** *Questions about sequential logic elements.*

(a) **[3 marks.]** This part is about the essential behaviour of a D latch. Complete the timing diagram.

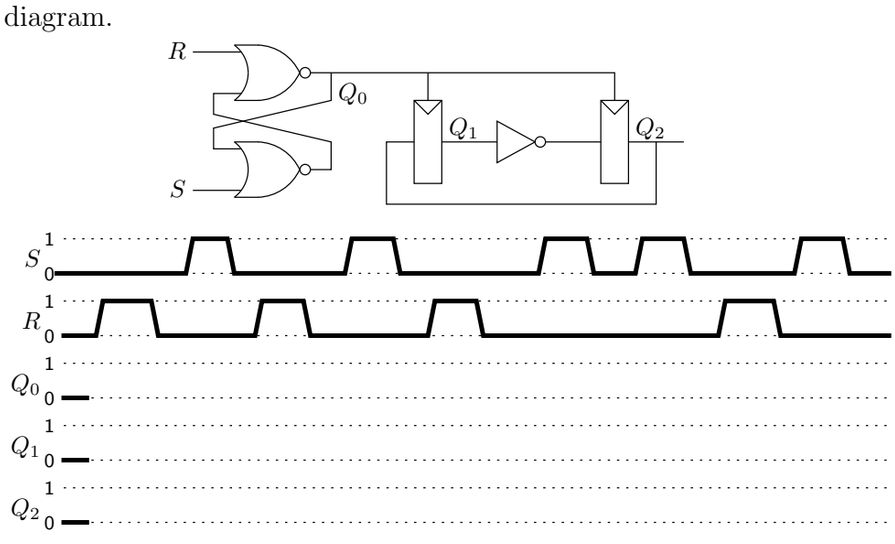


(b) **[4 marks.]** The 3-bit state register in the circuit below has an *asynchronous* reset input. Complete the timing diagram.



(c) **[3 marks.]** Usually the clock inputs of DFFs are driven by a periodic clock signal, but it's possible to build interesting DFF-based circuits with different kinds of clock connections.

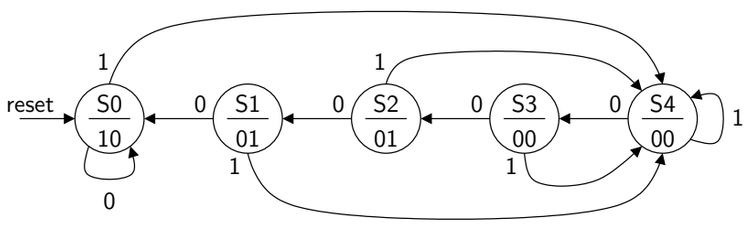
Assume, as shown, that $Q_0 = 0$, $Q_1 = 0$, and $Q_2 = 0$ at the beginning of the time interval in the given timing diagram. Complete the timing diagram.



6. **[13 marks total.]** *Questions on design of finite state machines (FSMs).*

   (a) **[5 marks.]** Consider an FSM with 1-bit input A and 1-bit output Y, such that $Y = 1$ if and only if one or the other of the following is true: (1) At the last 4 rising edges of the clock, A has been 0 (least recent), 1, 1, 0 (most recent); or (2) at the last 5 rising edges of the clock, A has been 0 (least recent), 1, 1, 1, 0 (most recent). Decide whether the FSM is Moore- or Mealy-type, then draw a state transition diagram.

   (b) **[8 marks.]** The FSM in this part is *unrelated* to the FSM of part (a). It has a 1-bit system input A and a 2-bit system output $Y_{1:0}$. Given the following state transition diagram and state encoding, find minimal SOP expressions for next-state and output logic. Your solutions should take advantage of the don't-care outputs given in the truth table.

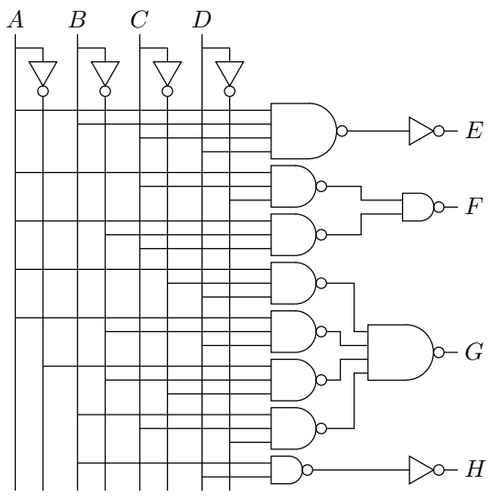


NAME	ENCODING $S_{2:0}$
S0	000
S1	011
S2	010
S3	110
S4	111

0	0	0	0			
0	0	0	1			
0	0	1	0	X	X	X
0	0	1	1	X	X	X
0	1	0	0			
0	1	0	1			
0	1	1	0			
0	1	1	1			
1	0	0	0	X	X	X
1	0	0	1	X	X	X
1	0	1	0	X	X	X
1	0	1	1	X	X	X
1	1	0	0			
1	1	0	1			
1	1	1	0			
1	1	1	1			

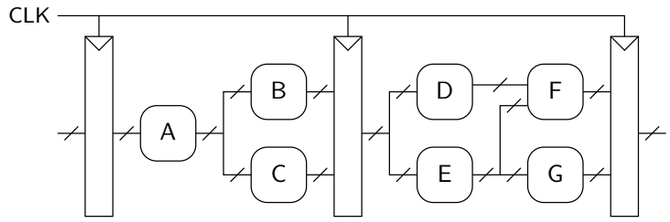
7. **[11 marks total.]** *Questions about timing.*

(a) **[3 marks.]** Determine overall t_{pd} and t_{cd} values for the given circuit. Show your work in the space below the table of timing parameters.



gate	t_{pd}	t_{cd}
NOT	16 ps	11 ps
NAND2	30 ps	17 ps
NAND3	44 ps	24 ps
NAND4	58 ps	32 ps

(b) **[3 marks.]** The synchronous sequential system shown below is to run with a clock frequency of 2.50 GHz. Five of the seven combinational elements have been designed and have the timing parameters given in the table. For the registers, $t_{pcq} = 40$ ps and $t_{setup} = 21$ ps. Find maximum allowable values of t_{pd} for elements A and F, assuming that there is zero clock skew.

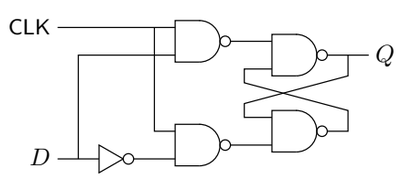


element	t_{pd}
B	250 ps
C	230 ps
D	112 ps
E	123 ps
G	134 ps

(c) **[2 marks.]** Find maximum allowable values of t_{pd} for elements A and F in part (b), assuming that there is clock skew of 25 ps.

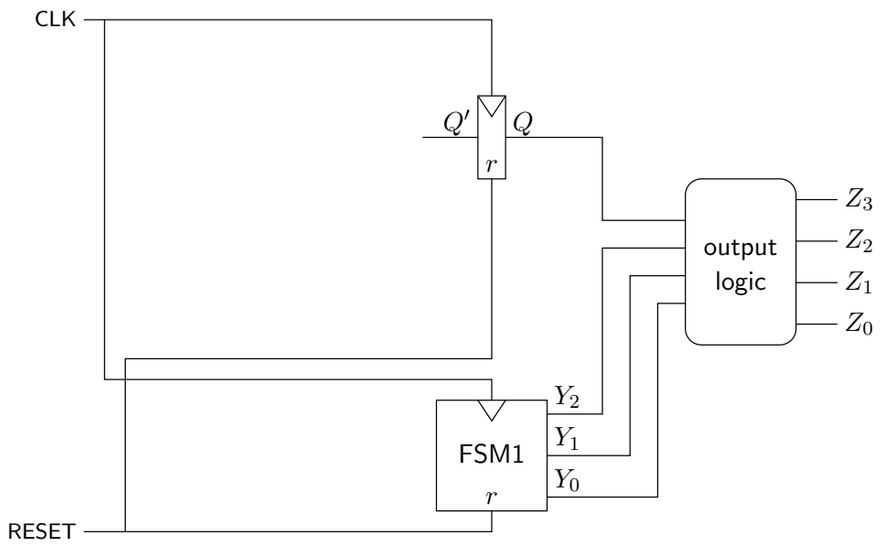
(d) **[3 marks.]** ENEL 353 did not present the concept of timing parameters for a D latch, but such parameters are similar in some ways to D flip-flop timing parameters. For a D latch, t_{ccq} is the shortest possible delay between a rising edge of the clock and a change in the output Q, and t_{pcq} is the longest possible such delay. For both parameters, it's assumed that the D input does not change close in time to the rising edge of the clock.

For the given NAND-based D latch, determine t_{ccq} and t_{pcq}, using timing parameters from part (a). (Hint: Consider how the circuit will behave in these two cases: $(D, Q) = (0, 1)$ before CLK goes $0 \to 1$; $(D, Q) = (1, 0)$ before CLK goes $0 \to 1$.)



8. **[8 marks.]** The components in the incomplete schematic below are a DFF with synchronous reset, an FSM, and a yet-to-designed "output logic" component.

   When RESET is 1, the FSM1 output $Y_{2:0}$ goes to 000 on the next rising edge of CLK. When RESET is 0, $Y_{2:0}$ cycles through the sequence 000, 001, 010, 011, 100, 000, 001, and so on, with updates once per clock cycle.

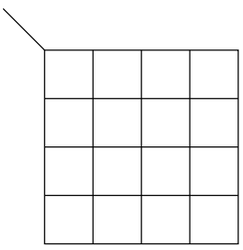


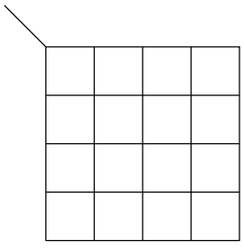
   The overall system output $Z_{3:0}$ should go to 0000 when RESET is 1, and should cycle through this ten-value sequence when RESET is 0:

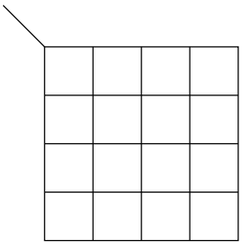
   0000, 0001, 0011, 0010, 0110, 1110, 1010, 1011, 1001, 1000, 0000, 0001, ...

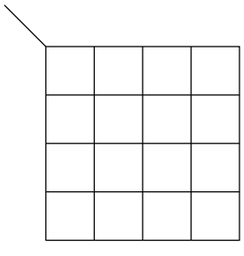
   Add wires and one or more logic gates to the schematic to drive Q', the DFF input, and write minimal SOP expressions for the "output logic" circuit. The given blank truth table and K-maps should be helpful in solving the problem.

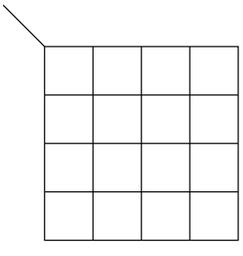
0	0	0	0	
0	0	0	1	
0	0	1	0	
0	0	1	1	
0	1	0	0	
0	1	0	1	
0	1	1	0	
0	1	1	1	
1	0	0	0	
1	0	0	1	
1	0	1	0	
1	0	1	1	
1	1	0	0	
1	1	0	1	
1	1	1	0	
1	1	1	1	







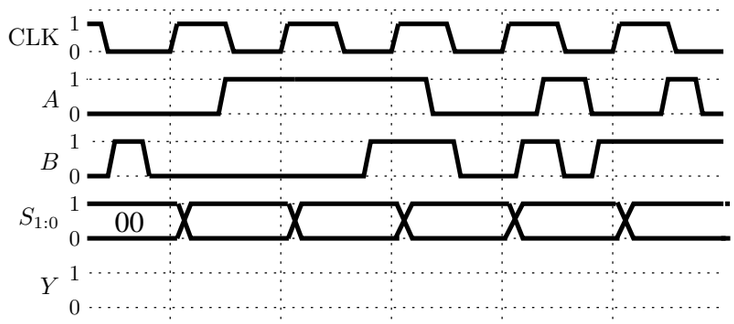




9. **[12 marks total.]** *Questions about FSM analysis.*

(a) **[4 marks.]** Below is the combined state and output table for a FSM that has two inputs A and B, and one output Y. The state variables are $S_{1:0}$. Use this table to complete the timing diagram.

$S_{1:0}$	AB	$S'_{1:0}$	Y	$S_{1:0}$	AB	$S'_{1:0}$	Y
00	00	00	0	01	1x	10	0
00	x1	10	1	10	x0	11	1
00	10	01	0	10	01	10	0
01	00	00	1	10	11	01	1
01	01	01	0	11	xx	00	0



(b) **[8 marks.]** Consider the FSM sketched below. There is one input A, and one output Y. Determine the combined state and output table, and sketch the state-transition diagram. In your table, use 0's and 1's for the states and next states, not symbols like S0, S1, etc.