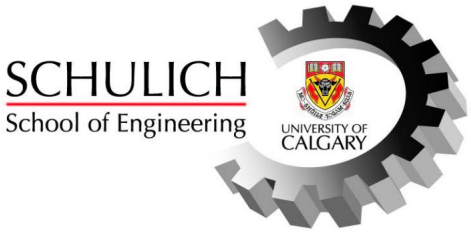
Name: _____ Lecture Section: _____

L01 – Norm Bartley, lectures in ENE 241
L02 – Steve Norman, lectures in ST 145



DEPARTMENT OF ELECTRICAL
AND COMPUTER ENGINEERING

ENEL 353 - Digital Circuits

Midterm Examination

Wednesday, October 29, 2014

Instructions:

- Time allowed is 90 minutes.
- In order to minimize distraction to your fellow students, you may not leave during the last 10 minutes of the examination.
- The examination is closed-book.
- Non-programmable calculators are permitted.
- The maximum number of marks is 50, as indicated; the midterm examination counts 20% toward the final grade.
- Please use a pen or heavy pencil to ensure legibility.
- Please answer questions in the spaces provided; if space is insufficient, please use the back of the pages.
- Please show your work; where appropriate, marks will be awarded for proper and well-reasoned explanations.

UCID: _____

1. **[12 marks total.]**

   (a) **[3 marks.]** Use repeated division to convert 571_{10} to hexadecimal.

   (b) **[1 mark.]** What is the value of 417_8 as a decimal number?

   (c) **[2 marks.]** The eight-bit two's complement representation of -121_{10} is 10000111. Use this information to find the eight-bit two's complement representation of $+121_{10}$.

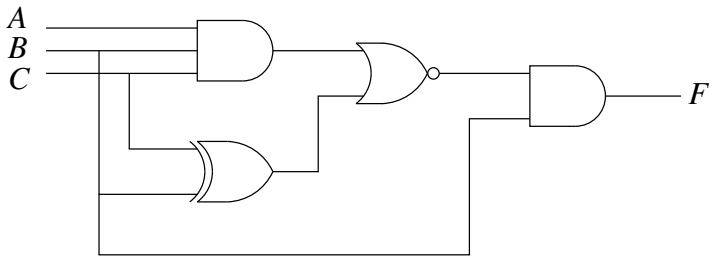
   (d) **[2 marks.]** Represent the number $+67_{10}$ in eight-bit *sign-and-magnitude* format.

   (e) **[2 marks.]** What is the five-bit sum generated by a five-bit adder when the inputs are 01011 and 01001, and what is the carry out of the most significant bit?

   (f) **[1 mark.]** If all the five-bit numbers in part (e) are interpreted as two's-complement, was there overflow in the addition? Give a reason for your answer.

   (g) **[1 mark.]** If all the five-bit numbers in part (e) are interpreted as unsigned, was there overflow in the addition? Give a reason for your answer.

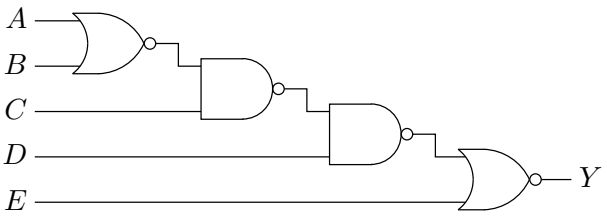
2. **[5 marks.]** Consider the circuit below.



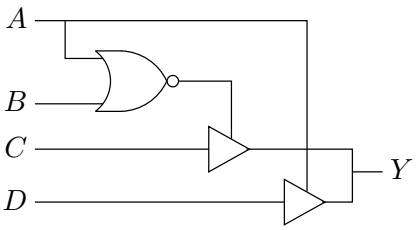
Let $G = \bar{A}BC$. By *algebraic manipulation*, prove or disprove that $F = G$. (Do not use a truth table or a K-map.)

3. **[8 marks total.]**

(a) **[3 marks.]** Use "bubble-pushing" and/or algebra to find an SOP expression for the function implemented by the circuit below. Use the space beside and below the circuit to show your work.



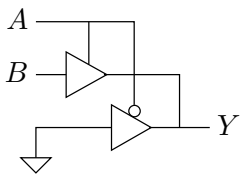
(b) **[3 marks.]** The circuit below is built from two tristate buffers and a NOR gate.



Is it possible to choose 0 or 1 values for the inputs that result in contention (also known as "fighting" at the output node Y)? Give a precise explanation for your answer.

Is it possible to choose 0 or 1 values for the inputs that result in Y being in the Z (floating, high-impedance)? Give a precise explanation for your answer.

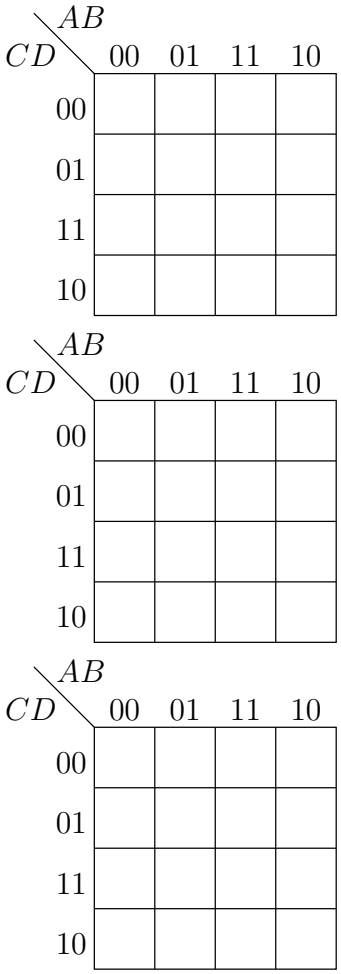
(c) **[2 marks.]** The circuit below uses two tristate buffers, one with active-high enable, and one with active-low enable. What simple logic function of A and B does the circuit implement? Give a reason for your answer.



4. **[11 marks total.]**

(a) **[8 marks.]** Consider the function Y given in the truth table below. Use the blank K-maps to derive *all* minimum SOP and POS expressions for Y. Indicate all essential prime implicants for Y or $\bar{Y}$ in your maps. You may add more maps if you need them.

A	B	C	D	Y
0	0	0	0	0
0	0	0	1	0
0	0	1	0	1
0	0	1	1	X
0	1	0	0	1
0	1	0	1	X
0	1	1	0	0
0	1	1	1	X
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	X
1	1	0	0	1
1	1	0	1	1
1	1	1	0	X
1	1	1	1	0



(b) **[3 marks.]** Sketch a two-level NAND-NAND circuit for a minimal SOP expression from part (a). If there is not a unique minimal SOP expression, state which one you are implementing. Inputs are available in both true and complementary forms. Any number of inputs are allowed on each NAND gate.

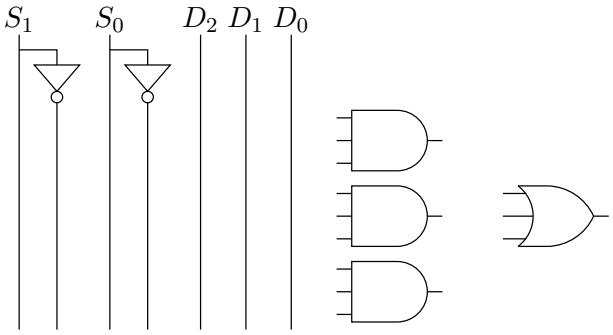
5. **[9 marks total.]**

(a) **[3 marks.]** Draw a schematic to show how the function given in the truth table can be implemented with a 4:1 multiplexer, *one* inverter, and no other components. Show any intermediate work you had to do to design the circuit.

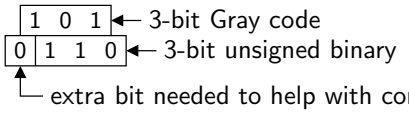
A	B	C	Y
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

(b) **[3 marks.]** A table describing a 3:1 multiplexer is given below to the left. Add wiring to show how this function can be implemented using two inverters, three 3-input AND gates, and one 3-input OR gate.

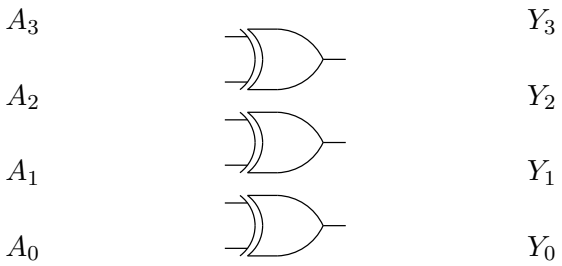
S_1	S_0	Y
0	0	D_0
0	1	D_1
1	0	D_2
1	1	D_2



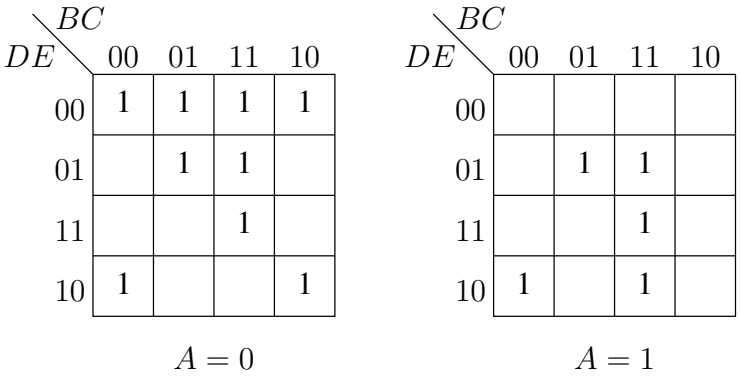
(c) **[3 marks.]** The diagram below is intended to serve as a reminder of how to convert between unsigned binary code and Gray code.



Add wiring to the following schematic so that the output $Y_3Y_2Y_1Y_0$ is the four-bit Gray code corresponding to the input unsigned binary number $A_3A_2A_1A_0$. You may wire things however you like, but you may not introduce any additional logic gates.



6. **[5 marks.]** Use the following 5-variable K-map for $F(A, B, C, D, E)$, and find any minimal SOP expression for F.



Name (printed):

U of Calgary ID number:

Section (L01 is in ENE 241 with Norm Bartley, L02 is in ST 145 with Steve Norman):

Problem	Mark
1	/ 12
2	/ 5
3	/ 8
4	/ 11
5	/ 9
6	/ 5
TOTAL	/ 50