Name: Solutions (revised)

Lecture Section: _____

L01 – Norm Bartley, lectures in ENE 241

L02 – Steve Norman, lectures in ST 145

SCHULICH School of Engineering

UNIVERSITY OF CALGARY

DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING

ENEL 353 - Digital Circuits

Midterm Examination

Wednesday, October 29, 2014

Instructions:

- Time allowed is 90 minutes.
- In order to minimize distraction to your fellow students, you may not leave during the last 10 minutes of the examination.
- The examination is closed-book.
- Non-programmable calculators are permitted.
- The maximum number of marks is 50, as indicated; the midterm examination counts 20% toward the final grade.
- Please use a pen or heavy pencil to ensure legibility.
- Please answer questions in the spaces provided; if space is insufficient, please use the back of the pages.
- Please show your work; where appropriate, marks will be awarded for proper and well-reasoned explanations.

UCID: _____

1. **[12 marks total.]**

(a) **[3 marks.]** Use repeated division to convert 571_{10} to hexadecimal.

division	quotient	remainder
$571 \div 16$	35	$11 = B_{16}$
$35 \div 16$	2	3
$2 \div 16$	0	2

Answer: $23B_{16}$

(b) **[1 mark.]** What is the value of 417_8 as a decimal number?

$4 \times 8^2 + 1 \times 8^1 + 7 \times 8^0 = 271_{10}$

(c) **[2 marks.]** The eight-bit two's complement representation of -121_{10} is 10000111. Use this information to find the eight-bit two's complement representation of $+121_{10}$.

invert bits: 0 111 1000
add 1: 1
answer 0111 1001

(d) **[2 marks.]** Represent the number $+67_{10}$ in eight-bit *sign-and-magnitude* format.

$67_{10} = 64 + 2 + 1$, so the magnitude is 1000011_2
The sign bit is 0, so the answer is 01000011

(e) **[2 marks.]** What is the five-bit sum generated by a five-bit adder when the inputs are 01011 and 01001, and what is the carry out of the most significant bit?

carries: 0 10110
01011
+ 01001
10100 ⇐ sum

carry out of MSB is 0.

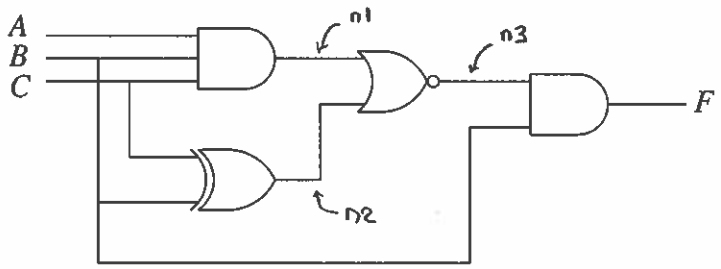
(f) **[1 mark.]** If all the five-bit numbers in part (e) are interpreted as two's-complement, was there overflow in the addition? Give a reason for your answer.

Yes. The sum of two positive numbers is negative.
Alternate reason: Carry out of MSB ≠ carry into MSB.

(g) **[1 mark.]** If all the five-bit numbers in part (e) are interpreted as unsigned, was there overflow in the addition? Give a reason for your answer.

No. The carry out from the MSB was 0.
Alternate reasons: (1) Sum ≥ 01011; (2) sum ≥ 01001.

2. **[5 marks.]** Consider the circuit below.



Let $G = \bar{A}BC$. By *algebraic manipulation*, prove or disprove that $F = G$. (Do not use a truth table or a K-map.)

At n_1, $n_1 = ABC$

At n_2, $n_2 = B \oplus C = \bar{B}C + B\bar{C}$

At n_3, $n_3 = (ABC + \bar{B}C + B\bar{C})$

And $F = \overline{(ABC + \bar{B}C + B\bar{C})}\,B$

De Morgan's theorem: $F = (\overline{ABC})(\overline{\bar{B}C})(\overline{B\bar{C}})\,B$

Again: $F = (\bar{A} + \bar{B} + \bar{C})\underbrace{(B + \bar{C})(\bar{B} + C)}$

$B\bar{B} + BC + \bar{B}\bar{C} + C\bar{C}$

$= BC + \bar{B}\bar{C}$

$F = (\bar{A} + \bar{B} + \bar{C})\underbrace{(BC + \bar{B}\bar{C})\,B}$

$BBC + B\bar{B}\bar{C} = BC$

$F = (\bar{A} + \bar{B} + \bar{C})(BC)$

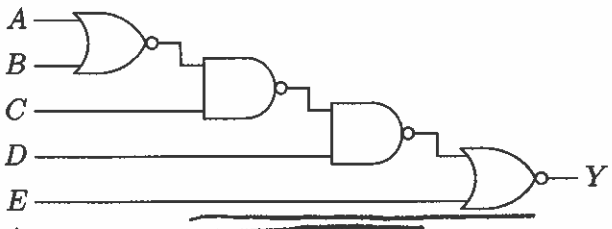
$= \bar{A}BC + \bar{B}BC + BC\bar{C}$

$= \bar{A}BC$

Thus, $F = G$.

3. **[8 marks total.]**

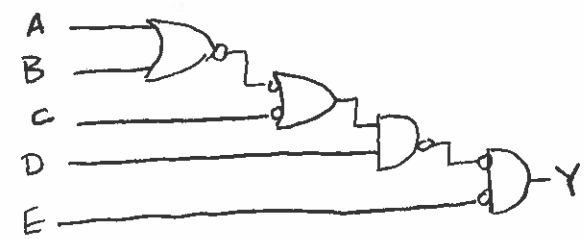
(a) **[3 marks.]** Use "bubble-pushing" and/or algebra to find an SOP expression for the function implemented by the circuit below. Use the space beside and below the circuit to show your work.



Algebra:

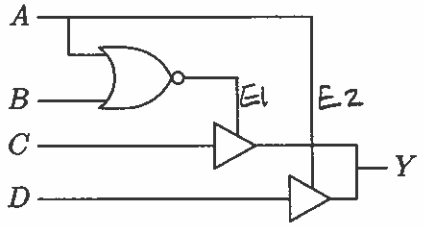
$$Y = \overline{(\overline{(A+B)}\cdot C)\cdot D} + E$$
$$= \overline{(A+B)}C + \overline{D} + E$$
$$= \overline{A}\,\overline{B}C + \overline{D} + E$$
$$= (A+B+\overline{C})D\overline{E}$$
$$= AD\overline{E} + BD\overline{E} + \overline{C}D\overline{E}$$

Bubble-pushing, then algebra



$$Y = (A+B+\overline{C})D\overline{E}$$
$$= AD\overline{E} + BD\overline{E} + \overline{C}D\overline{E}$$

(b) **[3 marks.]** The circuit below is built from two tristate buffers and a NOR gate.



A	B	$E1 = \overline{A+B}$	$E2 = A$
0	0	1	0
0	1	0	0
1	0	0	1
1	1	0	1

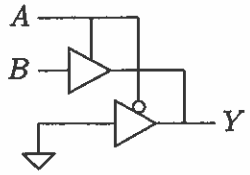
Is it possible to choose 0 or 1 values for the inputs that result in contention (also known as "fighting") at the output node Y? Give a precise explanation for your answer. No. The truth table shows that $E1 = 1$ and $E2 = 1$ can't both be true at the same time.

Is it possible to choose 0 or 1 values for the inputs that result in Y being in the Z (floating, high-impedance) state? Give a precise explanation for your answer.

Yes. If $A = 0$, $B = 1$, then neither tristate buffer is enabled.

Note: The above question text corrects some very minor typographical errors that appeared on the original question paper.

(c) **[2 marks.]** The circuit below uses two tristate buffers, one with active-high enable, and one with active-low enable. What simple logic function of A and B does the circuit implement? Give a reason for your answer.



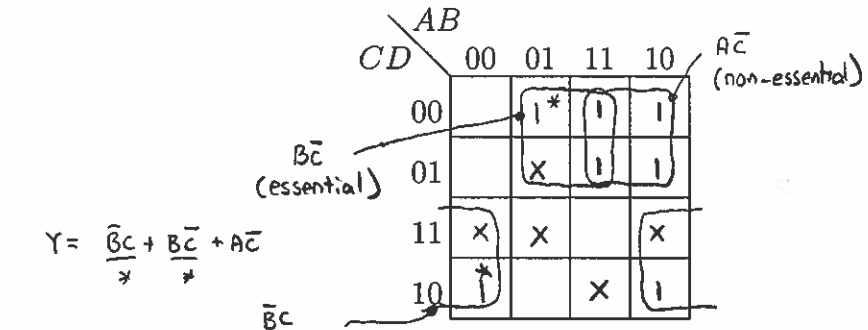
A	B	Y
0	0	0 (from GND)
0	1	0 (from GND)
1	0	0 (from B)
1	1	1 (from B)

The table shows that the circuit acts as an AND gate.

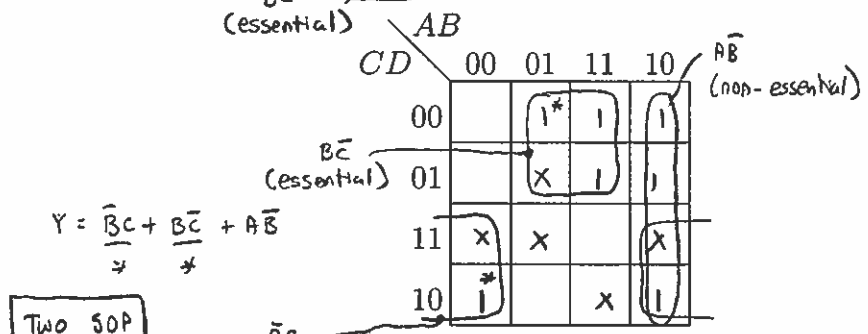
4. **[11 marks total.]**

(a) **[8 marks.]** Consider the function Y given in the truth table below. Use the blank K-maps to derive *all* minimum SOP and POS expressions for Y. Indicate all essential prime implicants for Y or $\bar{Y}$ in your maps. You may add more maps if you need them.

A	B	C	D	Y
0	0	0	0	0
0	0	0	1	0
0	0	1	0	1
0	0	1	1	X
0	1	0	0	1
0	1	0	1	X
0	1	1	0	0
0	1	1	1	X
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	X
1	1	0	0	1
1	1	0	1	1
1	1	1	0	X
1	1	1	1	0

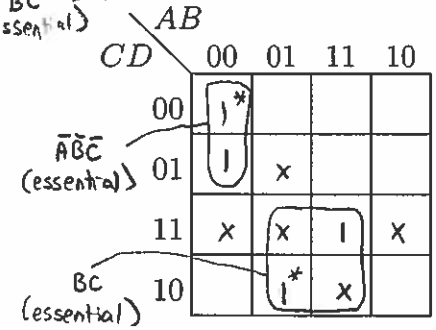


$Y = \bar{B}\bar{C} + B\bar{C} + A\bar{C}$



$Y = \bar{B}\bar{C} + B\bar{C} + A\bar{B}$

Two SOP solutions



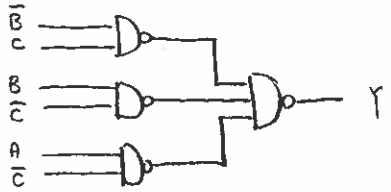
One POS solution

$\bar{Y} = \bar{A}\bar{B}\bar{C} + BC$

$Y = (A+B+C)(\bar{B}+\bar{C})$

(b) **[3 marks.]** Sketch a two-level NAND-NAND circuit for a minimal SOP expression from part (a). If there is not a unique minimal SOP expression, state which one you are implementing. Inputs are available in both true and complementary forms. Any number of inputs are allowed on each NAND gate.

Choose $Y = \bar{B}\bar{C} + B\bar{C} + A\bar{C} = \overline{(\bar{B}\bar{C})(B\bar{C})(A\bar{C})}$

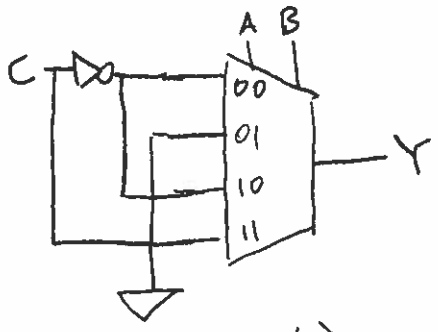


5. **[9 marks total.]**

(a) **[3 marks.]** Draw a schematic to show how the function given in the truth table can be implemented with a 4:1 multiplexer, *one* inverter, and no other components. Show any intermediate work you had to do to design the circuit.

A	B	C	Y	
0	0	0	1	$\overline{C}$
0	0	1	0	
0	1	0	0	0
0	1	1	0	
1	0	0	1	$\overline{C}$
1	0	1	0	
1	1	0	0	C
1	1	1	1	

A	B	Y
0	0	$\overline{C}$
0	1	0
1	0	$\overline{C}$
1	1	C



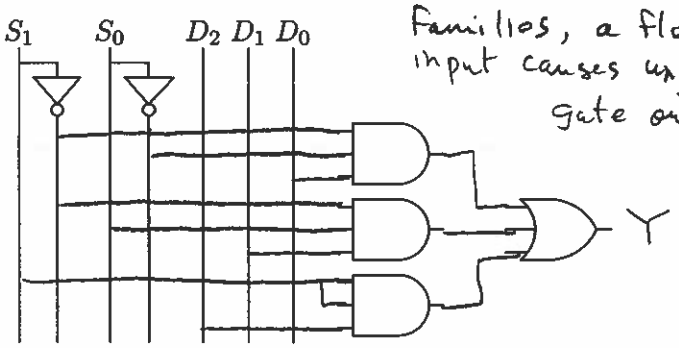
(Several other correct solutions exist.)

(b) **[3 marks.]** A table describing a 3:1 multiplexer is given below to the left. Add wiring to show how this function can be implemented using two inverters, three 3-input AND gates, and one 3-input OR gate.

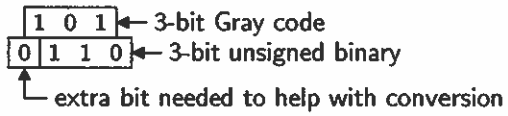
$Y = \overline{S}_1 \overline{S}_0 D_0 + \overline{S}_1 S_0 D_1 + S_1 D_2$

Note: In most logic families, a floating input causes unpredictable gate output.

S_1	S_0	Y
0	0	D_0
0	1	D_1
1	0	D_2
1	1	D_2



(c) **[3 marks.]** The diagram below is intended to serve as a reminder of how to convert between unsigned binary code and Gray code.



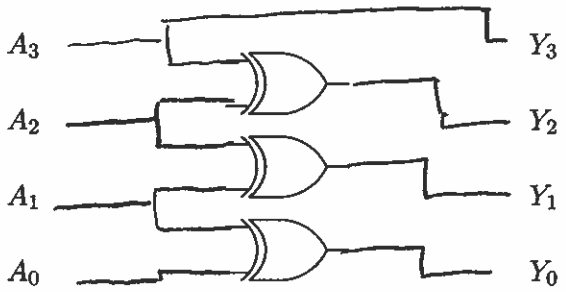
For 4 bits

Y_3	Y_2	Y_1	Y_0
0	A_3	A_2	A_1	A_0

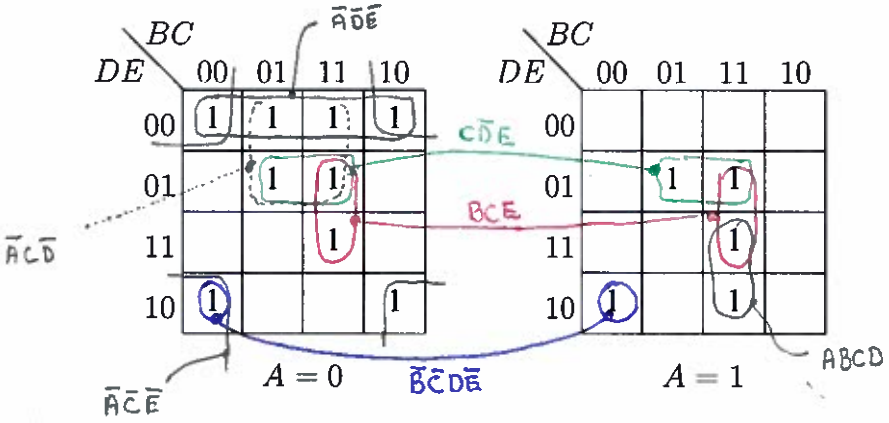
Add wiring to the following schematic so that the output $Y_3Y_2Y_1Y_0$ is the four-bit Gray code corresponding to the input unsigned binary number $A_3A_2A_1A_0$. You may wire things however you like, but you may not introduce any additional logic gates.

Y_2, Y_1, Y_0 are all XORs of adjacent bits within $A_{3:0}$.

$Y_3 = 0 \oplus A_3 = A_3$



6. **[5 marks.]** Use the following 5-variable K-map for $F(A, B, C, D, E)$, and find any minimal SOP expression for F.



Either of two solutions acceptable :

$$F = \bar{A}\bar{D}\bar{E} + \bar{A}\bar{C}\bar{E} + ABCD + C\bar{D}E + BCE + \bar{B}\bar{C}D\bar{E}$$

or $$F = \bar{A}C\bar{D} + \bar{A}\bar{C}\bar{E} + ABCD + C\bar{D}E + BCE + \bar{B}\bar{C}D\bar{E}$$

Name (printed):

U of Calgary ID number:

Section (L01 is in ENE 241 with Norm Bartley, L02 is in ST 145 with Steve Norman):

Problem	Mark
1	/ 12
2	/ 5
3	/ 8
4	/ 11
5	/ 9
6	/ 5
TOTAL	/ 50