Lecture Section: _____

Student Name or **ID Number**

UNIVERSITY OF CALGARY

DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING

ENEL 353 - Digital Circuits

Midterm Examination

Thursday, November 4, 2004
Time: 5:00 - 6:30 PM

Instructions:

- Time allowed is 90 minutes.
- The examination is closed-book.
- Non-programmable calculators are permitted.
- The maximum number of marks is 40, as indicated; the midterm examination counts 15% toward the final grade.
- Please use a pen or heavy pencil to ensure legibility.
- Please answer questions in the spaces provided; if space is insufficient, please use the back of the pages.
- Please show your work; marks will be awarded for proper and well-reasoned explanations.

Name: _____, *ID:* _____

1. **[8 marks (2 marks each).]** Consider the following 8-bit binary codes stored in a register in your computer's CPU:

   (i) `0001 0101`
   (ii) `1001 0111`

   (a) Assuming these codes are in sign-magnitude format, give their values in decimal.

   (b) Assuming these are unsigned binary codes, convert them to unsigned octal numbers.

   (c) Assuming these are unsigned binary codes, convert them to unsigned decimal numbers.

   (d) For your answers to part (c), find the four-digit 10's-complement of each.

2. **[4 marks.]** Assume that the binary codes given in Problem 1 are now in 8-bit 2's-complement binary format. Perform 8-bit binary addition of these numbers, and express your answer in decimal. Explain whether or not overflow occurs.

3. **[4 marks.]** Assume that the binary codes given in Problem 1 are now in BCD format. Perform BCD addition of these numbers.

4. **[18 marks total.]** A Boolean function F of four variables x_1, x_2, x_3 and x_4, is given by the Karnaugh map:

$x_1x_2 \backslash x_3x_4$			
1	1	0	1
1	0	0	0
0	0	0	0
1	0	1	1

(a) **[2 marks.]** Find a minimal SOP algebraic expression using this map.

(b) **[2 marks.]** Find a minimal POS expression using this map.

(c) **[2 marks.]** Draw the logic diagram of an *OR-AND-INVERT* circuit implementation. OR and AND gates with three or more inputs are allowed. Inverters are available. *(Note: for this and all remaining parts of this problem, you may assume that the variables and their complements are available to your circuit.)*

(d) **[4 marks.]** Using logic-symbol transformations and circuit manipulation, implement whatever circuit you give in part (c) using 2-input NAND gates only. Inverters are *not* available.

(e) **[5 marks.]** Implement the logic function F using a 4-to-1 multiplexer. You may use any AND, OR, and NOT gates as necessary. *(Hint: you may use either truth table decomposition or Shannon's expansion theorem.)*

(f) **[3 marks.]** Implement the logic function F using 1-to-8 decoders. You may use any AND, OR, and NOT gates as necessary.

5. **[6 marks.]** Design a circuit with four inputs x_1, x_2, x_3, x_4 and a single output F. The output should be $F = 1$ in either of the following cases:

   - $x_1 = 0$ and we have an *odd* function of x_2, x_3, x_4;
   - $x_2 = 1$ and we have an *even* function of x_1, x_3, x_4.

   The only logic gates available are AND and XOR gates. They may have three or more inputs. Inverters are *not* available.